Digital Design Techniques for Dependable High Performance Computing

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Computer and System Engineering Ph.D. Final Discussion

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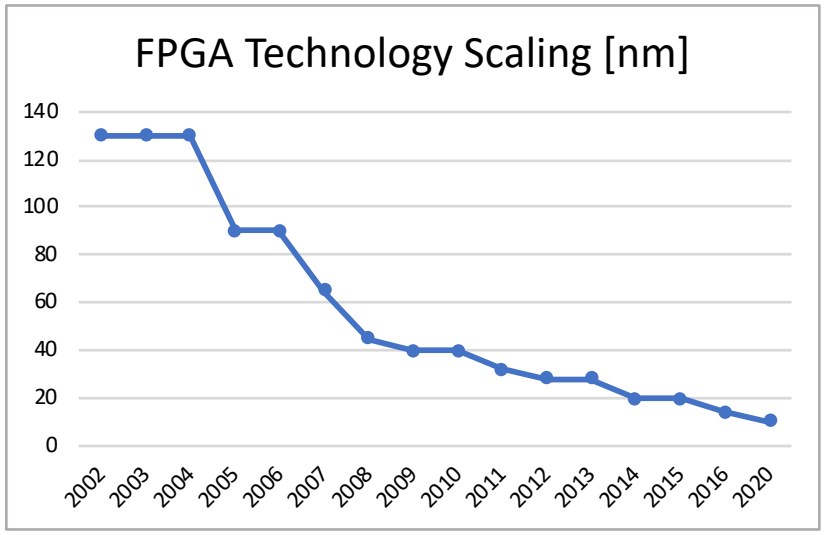
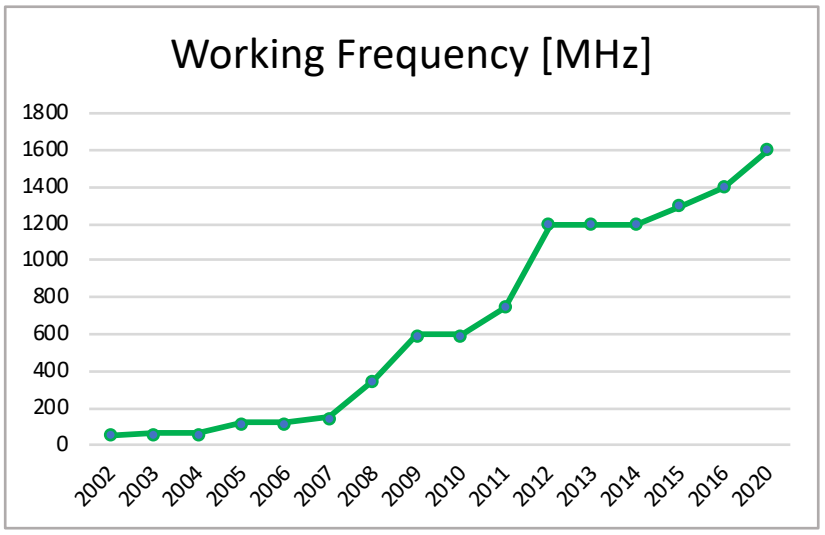
Motivation

- Dependability
  - Techniques to tolerate faults happening due to environment aspects, leading to the possible failure of the entire system
  - Radiation Effects
    - A set of particles interacting within the electronic system by an exchange of energy
- High Performance Computing
  - Technology scaling
  - Increasing of working frequency

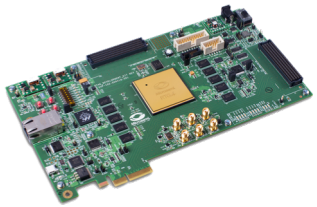




Motivation

- Dependability of High Performance Computing
  - Radiation Effects
    - Single Event Effects (SEE)
      - Single Event Upset (SEU)
      - Single Event Transient (SET)
      - Single Event Latch-up (SEL)
    - Total Ionizing Dose (TID)
    - Displacement Damage

Xilinx Kintex 7

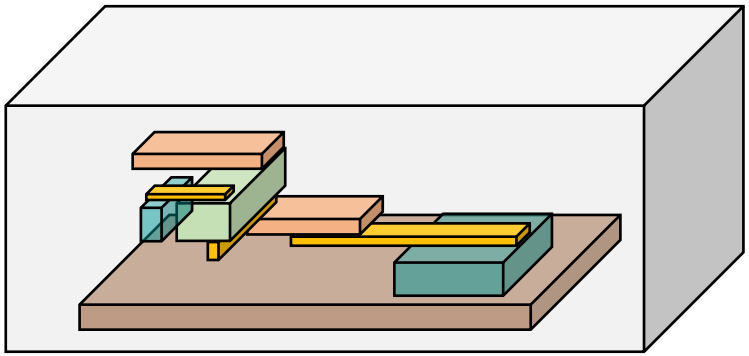


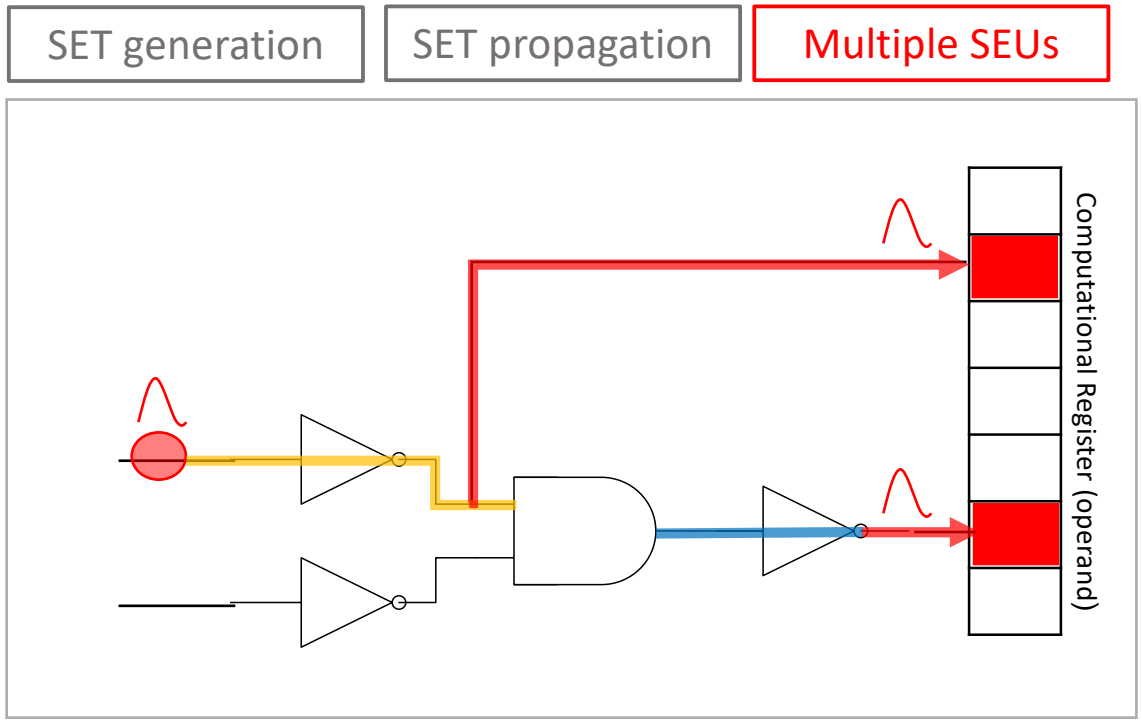
Microsemi RTG4

NVIDIA GPGPU

Single Event Transient

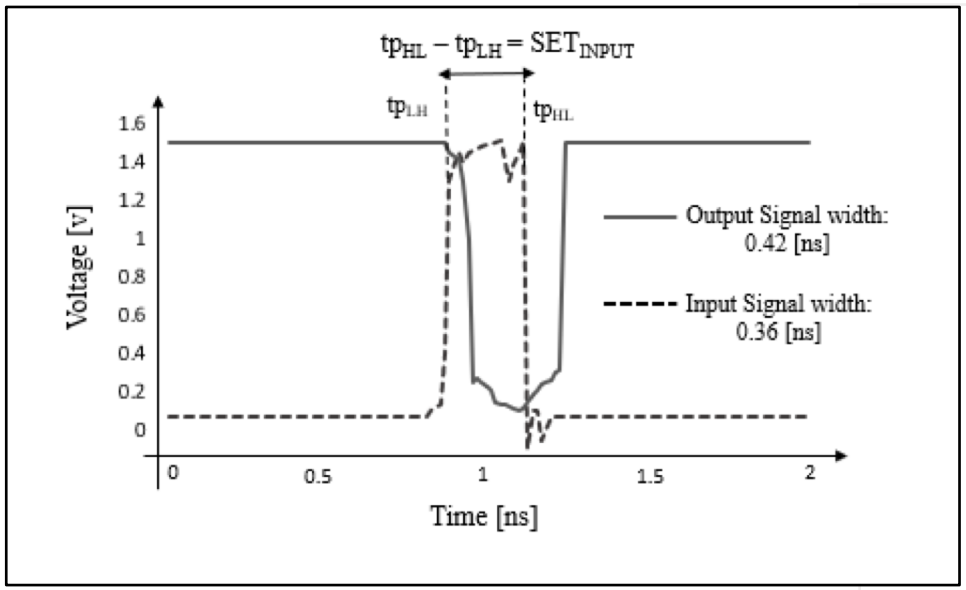
- Charge deposition and collection when a radiation particle strikes the layout structure
  - Generation of SET pulse
  - SET may propagate through multiple circuit paths
  - Generation of multiple SEUs in storage elements



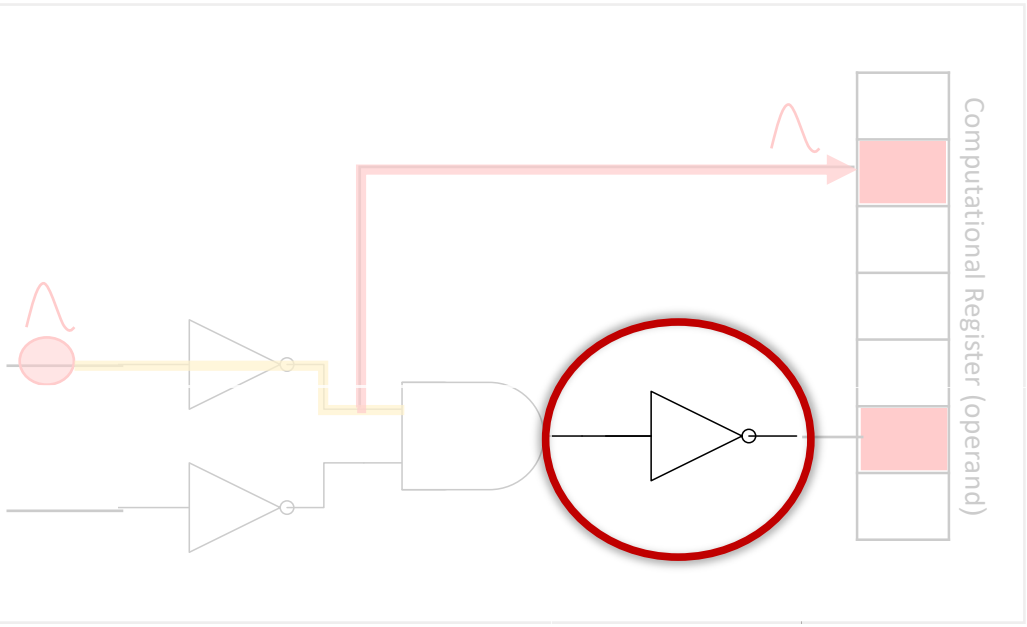


Single Event Transient

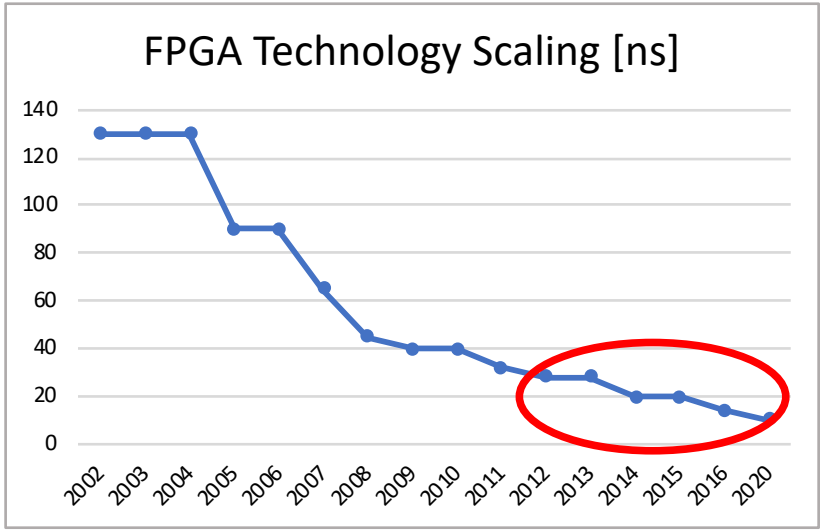
- SET pulse modification while traversing a logic gate
  - Propagation Induced Pulse Broadening (PIPB) Effect
  - Delay unbalance at different circuit nodes
  - Filtering or Broadening of SET pulses while traversing logic gates

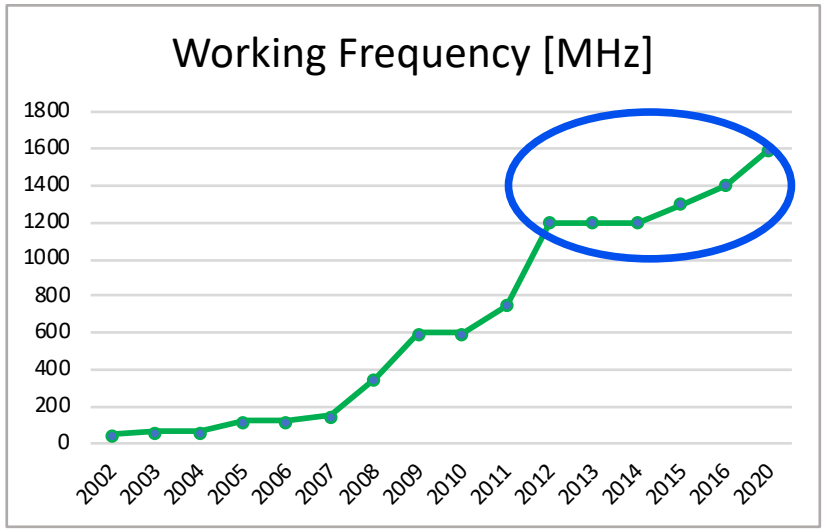


SET pulse traversing through an Inverter gate

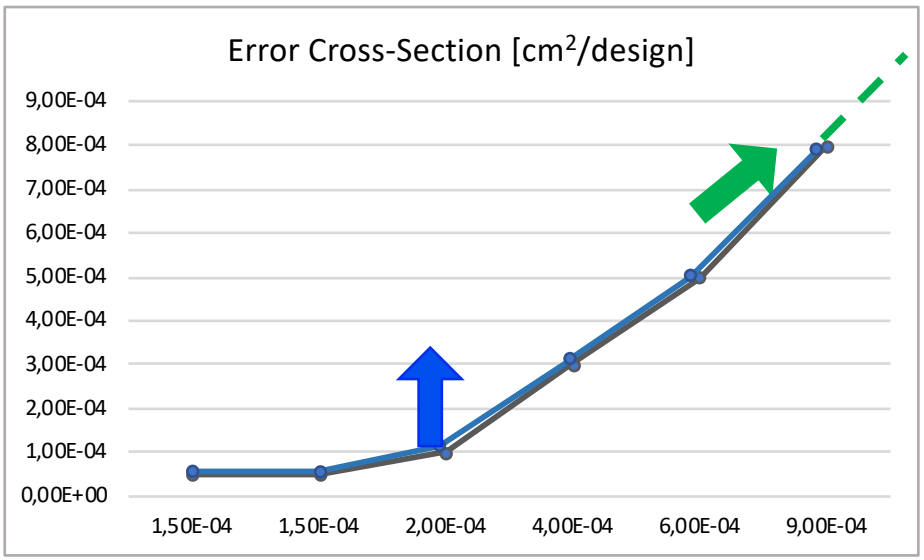


Single Event Transient





Low energy particle can cause change in the node voltage



Drastically increase of the sampling probablity of SET pulse

A. Dixit, A. Wood, "The impact of new technology on soft error rates", IEEE International Reliability Physics Symposium, 2011, pp. 5B.4.1- 5B.4.7.

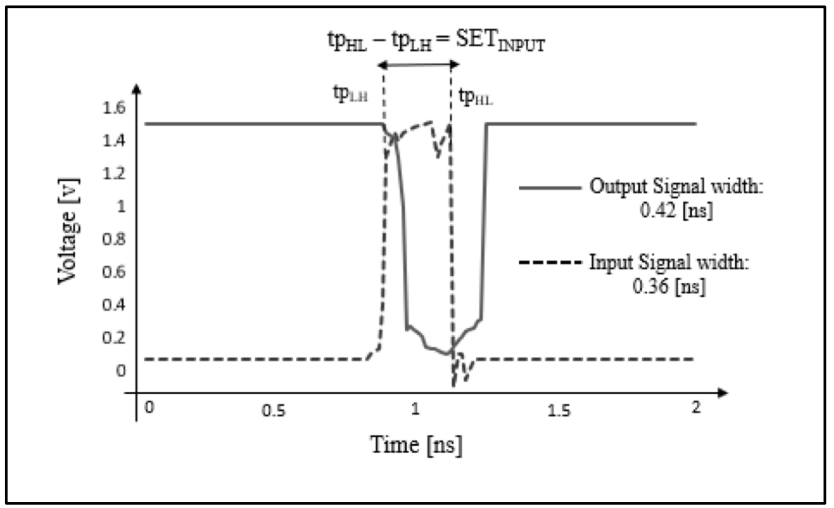
Scientific Advancement

Basic Mechanism	Application	Industrial
Modelization Characterization	Tools and Algorithms for Analysis and Mitigation	EUCLID Space Mission Project

Single Event Transient - Modeling

- Modeling of Single Event Transient phenomena focusing on:
  - Propagation Induced Pulse Broadening (PIPB) effect

1. $if\ \left(T_n < kt_p\right) \rightarrow T_{n+1} = 0$
2. $if\ \left(T_n < (k+3)t_p\right) \rightarrow T_{n+1} = T_n + \Delta t_p$
3. $if\ \left((k+1)t_p < T_n < (k+3)t_p\right) \rightarrow T_{n+1} = \frac{(T_n^2 - T_p^2)}{T_n} + \Delta t_p$
4. $if\ \left(kt_p < T_n < (k+1)t_p\right) \rightarrow T_{n+1} = (k+1)t_p\left(1 - e^{\left(k - \left({}^{T_n}/_{T_p}\right)\right)}\right) + \Delta t_p$

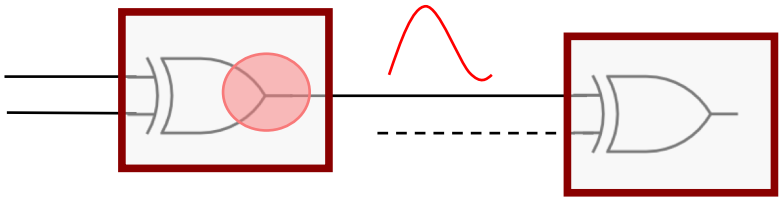


G. Wirth, F. Kastensmidt, I. Ribeiro , *"Single Event Transients in Logic Circuits—Load and Propagation Induced Pulse Broadening"*

L. Sterpone, B. Du, S. Azimi, "Radiation-induced single event transients modeling and testing on nanometric flash-based technologies", Microelectronic Reliability 2016

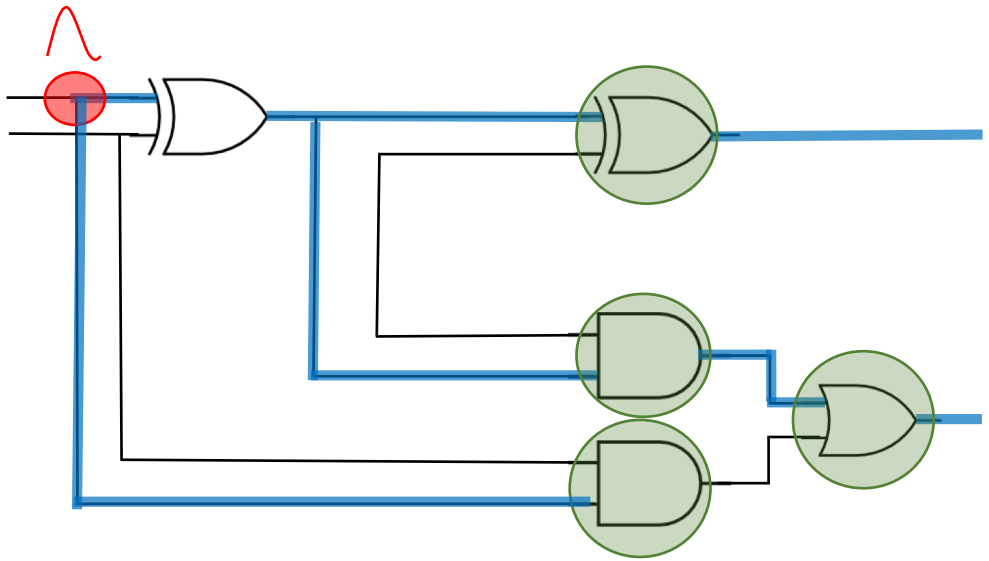
Single Event Transient - Characterization

- Nowadays investigations are focused on SET characterization between two gates



Single Event Transient - Characterization

- Focus of SET Characterization



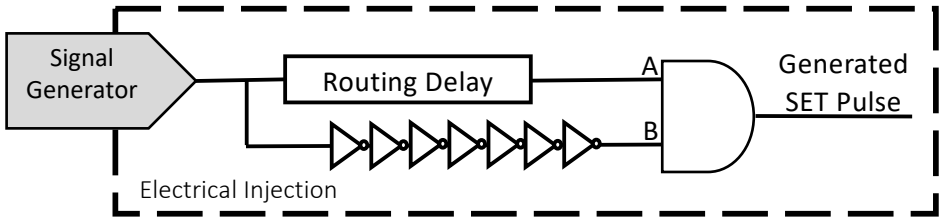
- Analysis of SET propagation through
  - Combinational logics
  - Routing resources

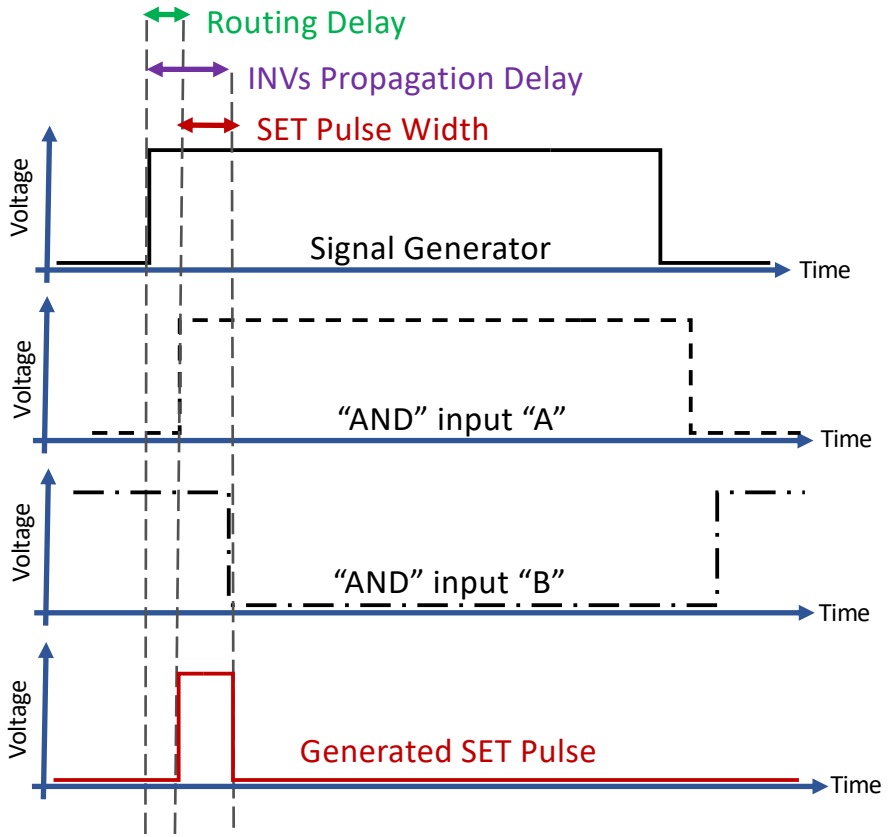
Single Event Transient

- Main methods to analyze SET pulses induced by particles striking the semiconductor of the devices
  - In-Circuit test
    - Emulation, fast, low-cost
  - Laser test
    - Emulation, precision
  - Radiation test
    - Accurate, expensive, not easy to analyze (mix of effects, SEU, SET)

Single Event Transient - In Circuit Test

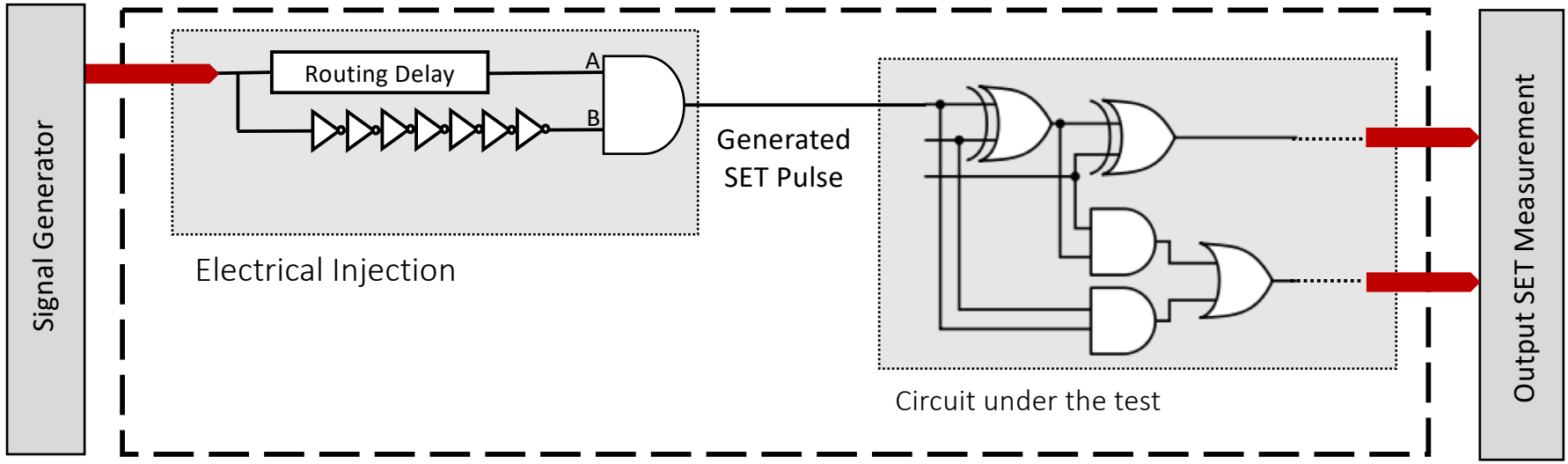
- In-Circuit Test generated pulse depends on:
  - Routing Delay
  - Inverters Propagation time





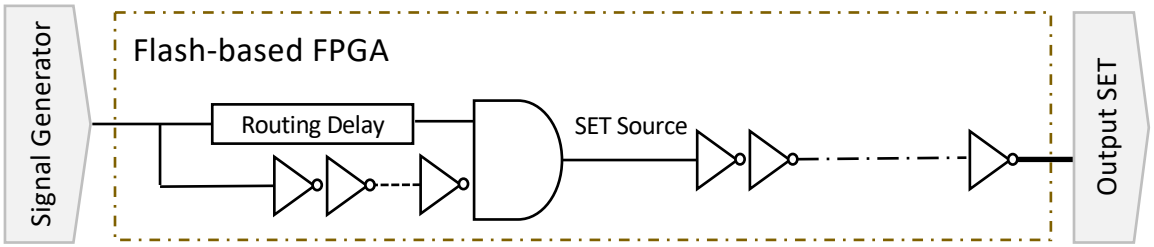
Single Event Transient - Characterization

- Developed methodology for SET characterization
  - Flash-based FPGA
  - SRAM-based FPGA

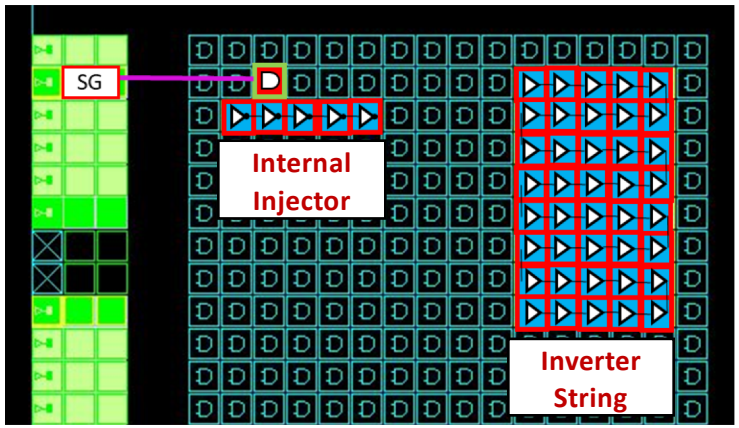


Single Event Transient - Characterization

- Circuit under the test considering four different scenarios
  - String of logic gates
  - String of logic gates with fan-out
  - Divergence path
  - Convergence path

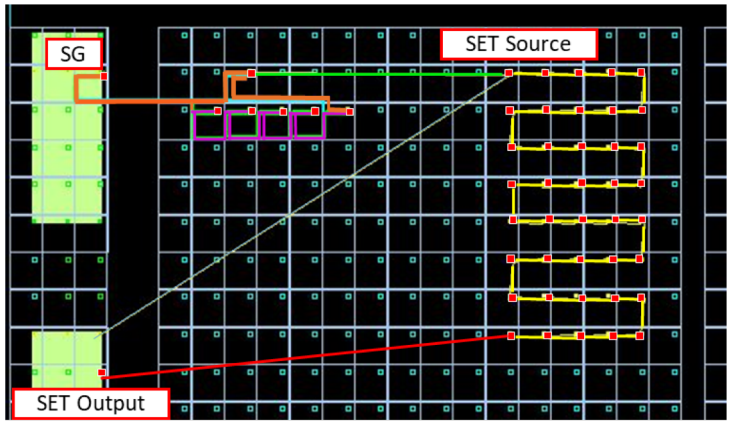


Placed side by side



Microsemi Libero SoC Commercial Design Tool
Placement

Minimal distance between each versatile



Microsemi Libero SoC Commercial Design Tool
Routing

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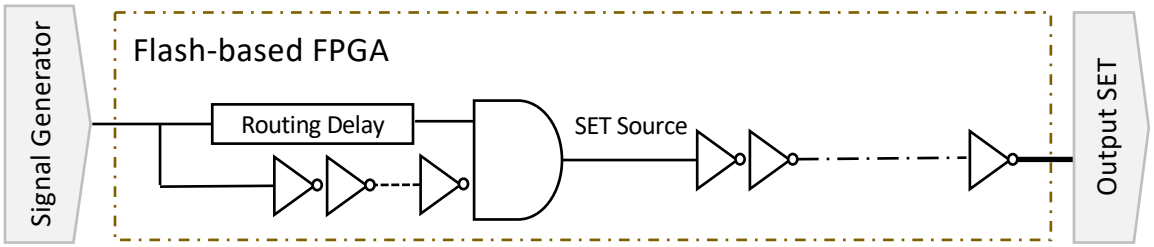
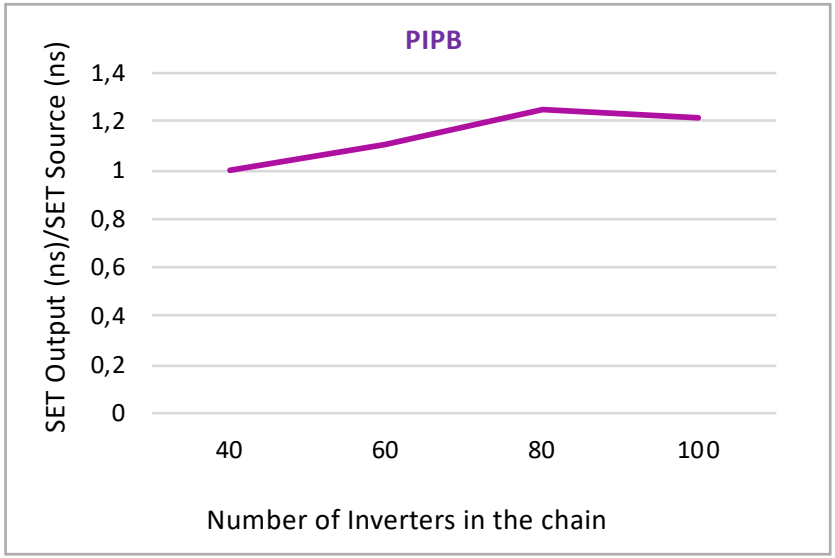
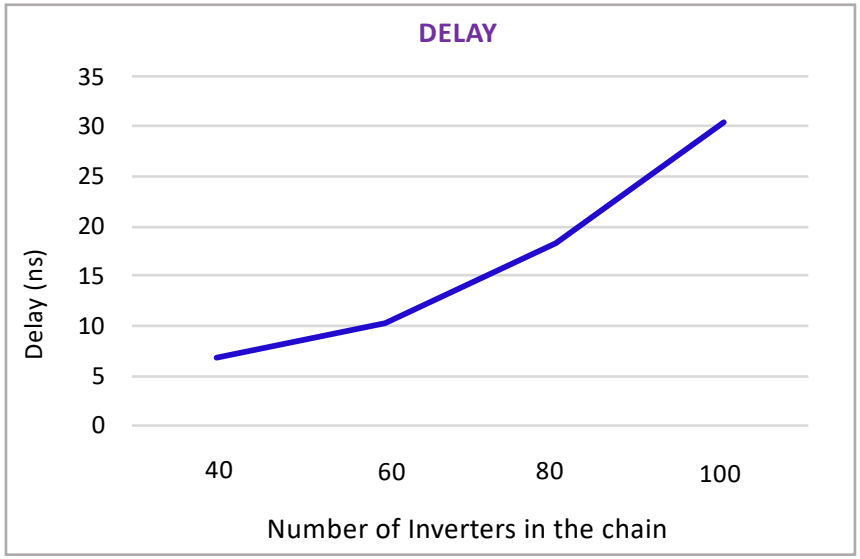


Increasing of PIPB when increasing the chain length



Increasing of delay when increasing the chain length



Sterpone, L, **Azimi, S**, "*Effective Characterization of Radiation-induced SET on Flash-based FPGAs*" , Radiation Effects on Components & Systems Conference (RADECS), 2017.

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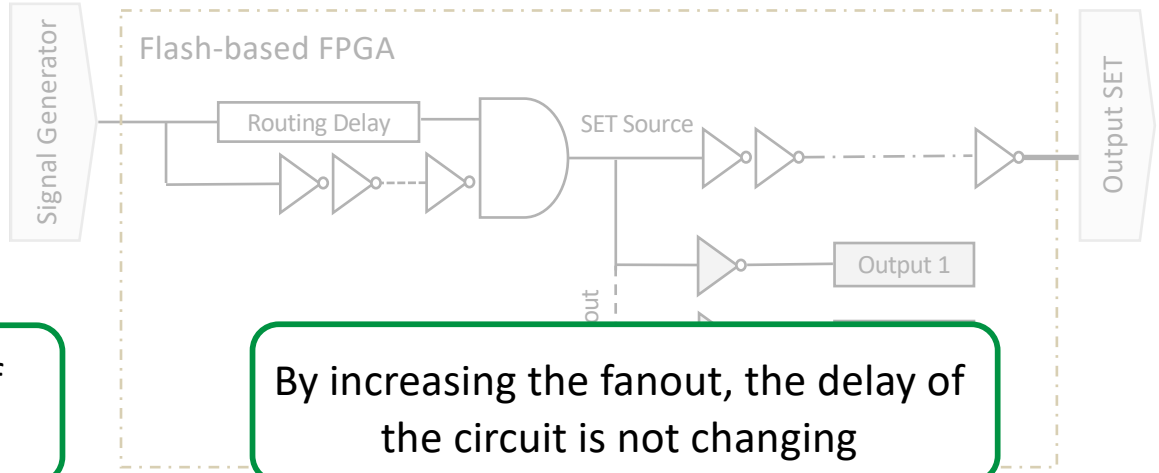
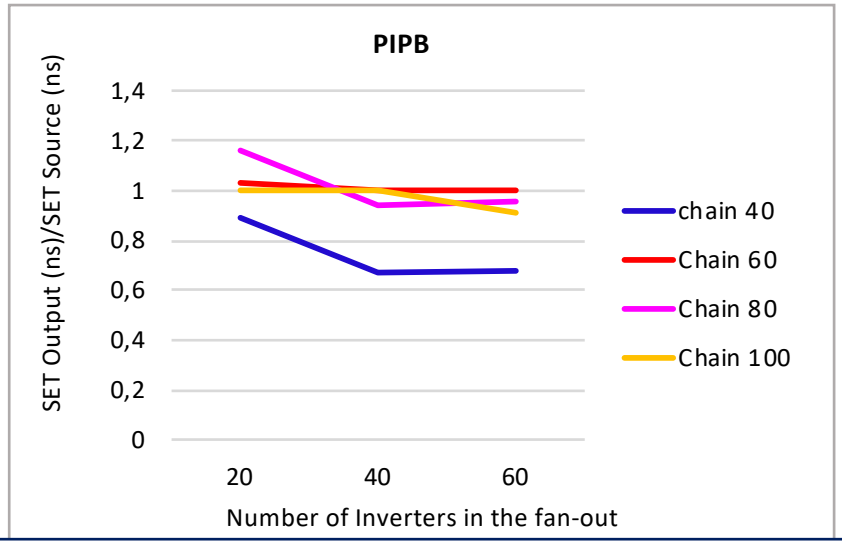
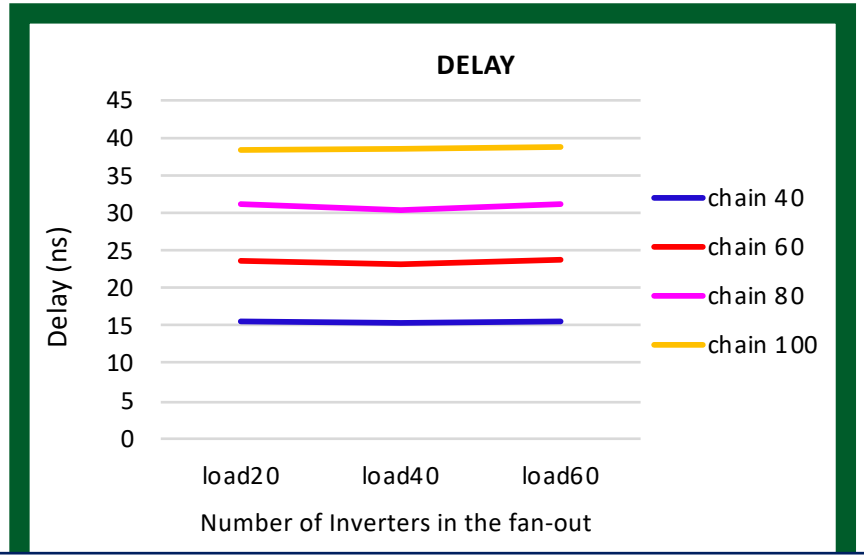


Attenuating of PIPB by increasing of Fanout

By increasing the fanout, the delay of the circuit is not changing





Sterpone. L, **Azimi. S**, "*Radiation-induced SET on Flash-based FPGAs: Analysis and Filtering methods*" ,Architecture of Computing Systems (ARCS) , 2017.

Single Event Transient - Characterization

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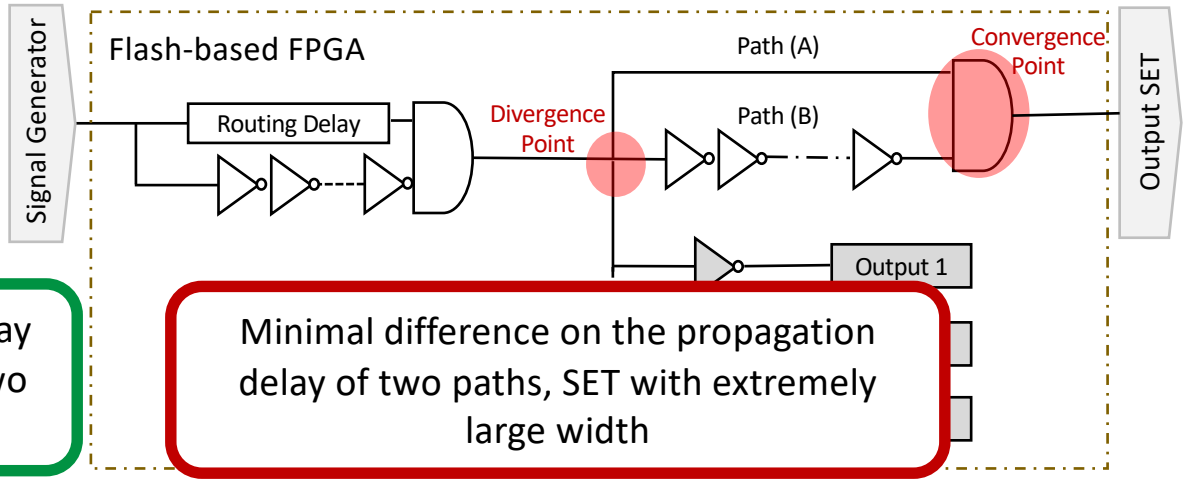
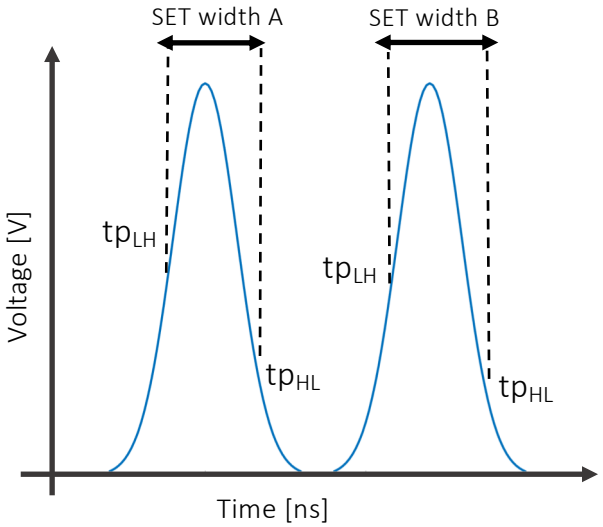
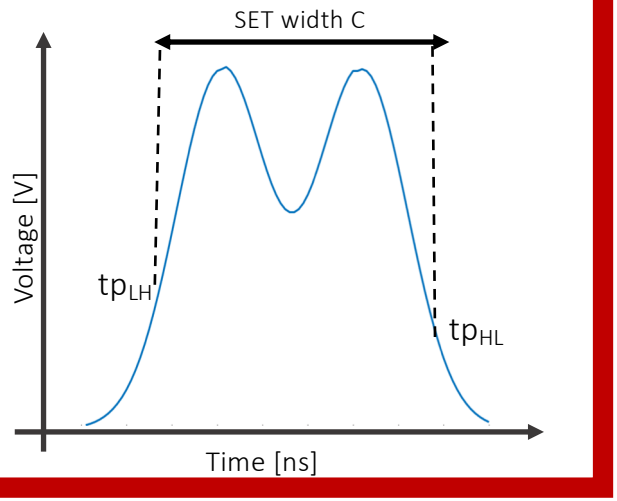


Large difference on the propagation delay of two paths, final SET is observed as two separate pulses

Minimal difference on the propagation delay of two paths, SET with extremely large width





Scientific Advancement

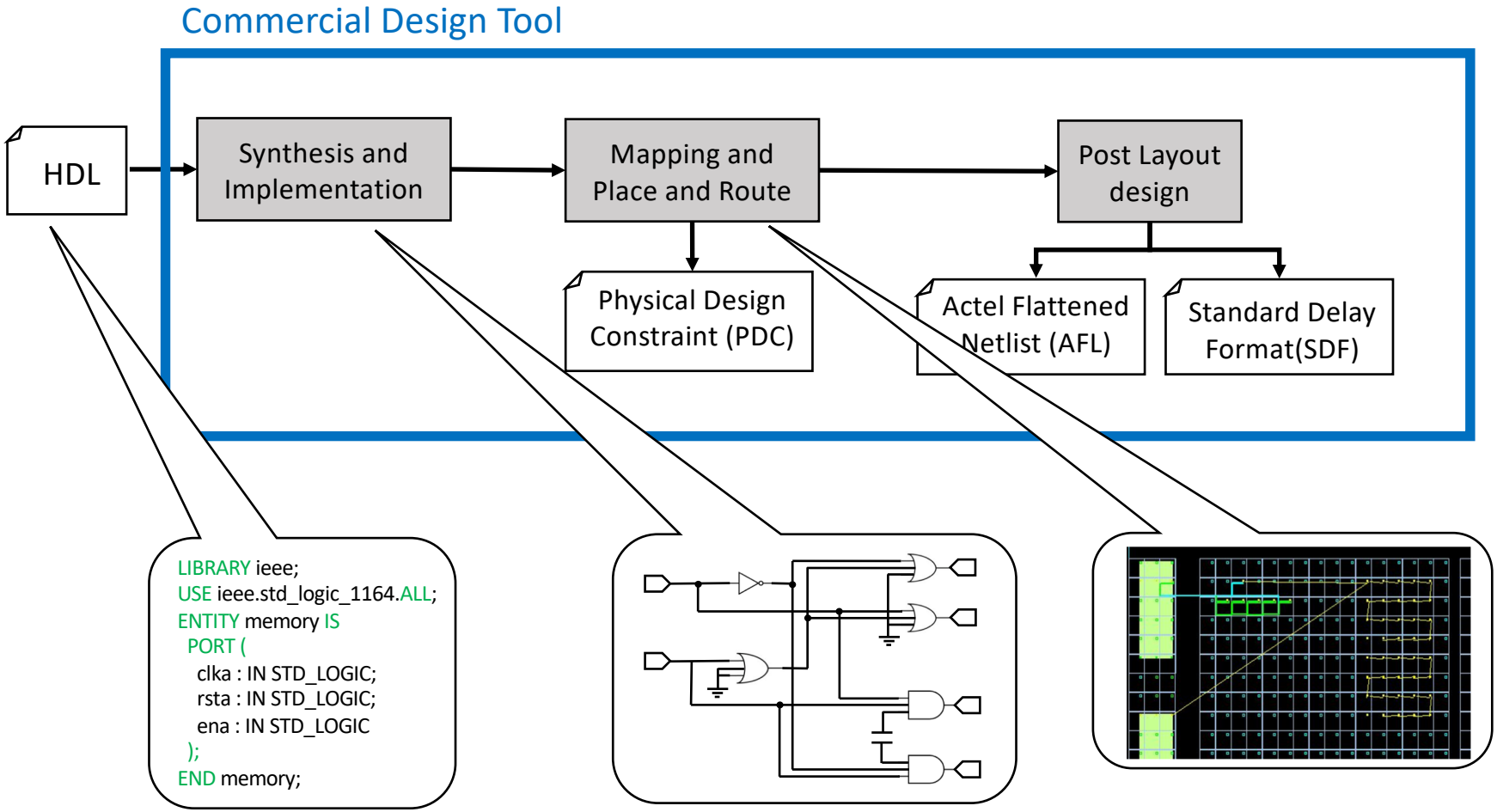
Basic Mechanism	Application	Industrial
Modelization Characterization	Tools and Algorithms for Analysis and Mitigation	EUCLID Space Mission Project

Single Event Transient Analyzer- SETA

- SETA: A developed CAD tool for evaluating the impact of SET on circuit functionality
- C-SETA: A developed CAD tool for evaluating the sensitivity of the implemented circuit regarding Convergence-SET
  - Targeting the PIPB effect
  - Applicable to large scale designs
  - Interfaceable with the commercial tool

Single Event Transient Analyzer- SETA

- SETA: A developed CAD tool for evaluating the impact of SET on circuit functionality



Single Event Transient Analyzer- SETA

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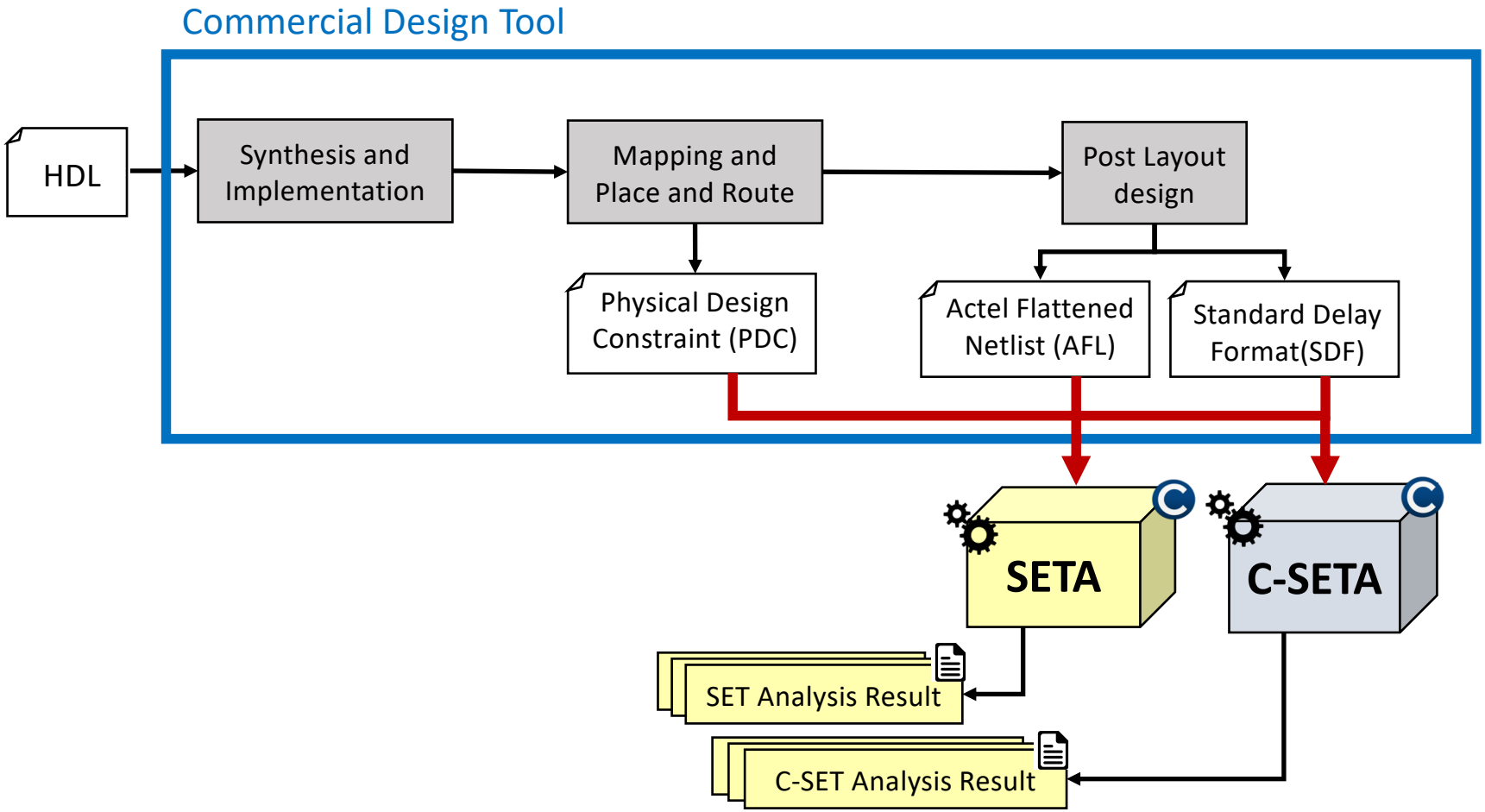
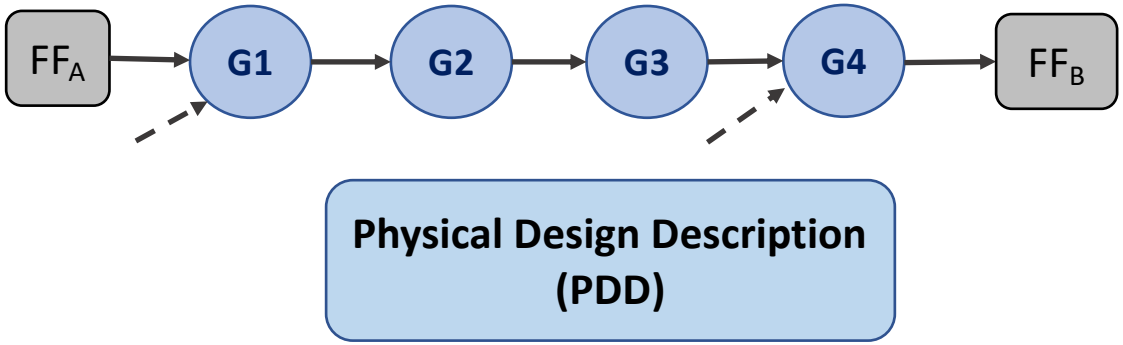
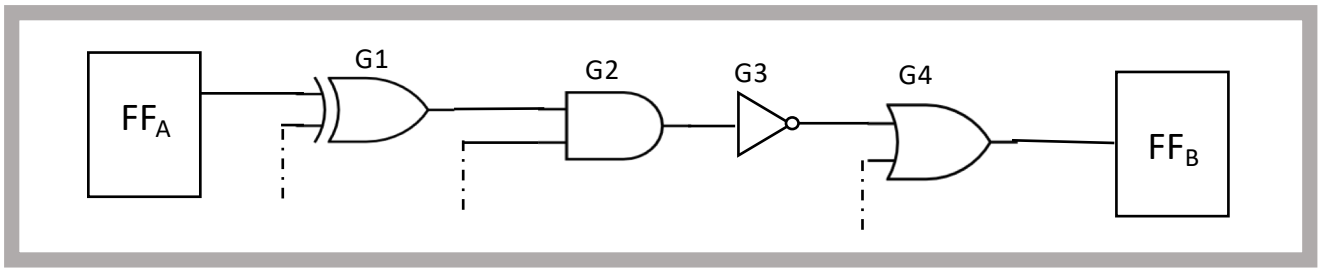


Azimi. S, Du. B, Sterpone. L, Codinachs, D. M, Cattaneo. L, "*SETA: A CAD Tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs*", Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD),

Single Event Transient Analyzer- SETA

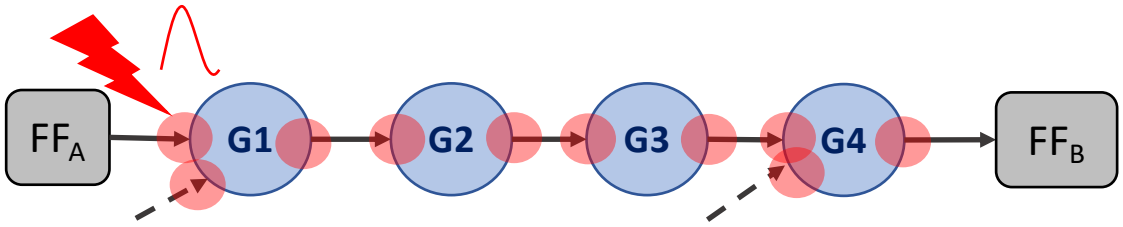
- SETA tool phases:
- Load circuit nodes
  - Logic Functions and FFs



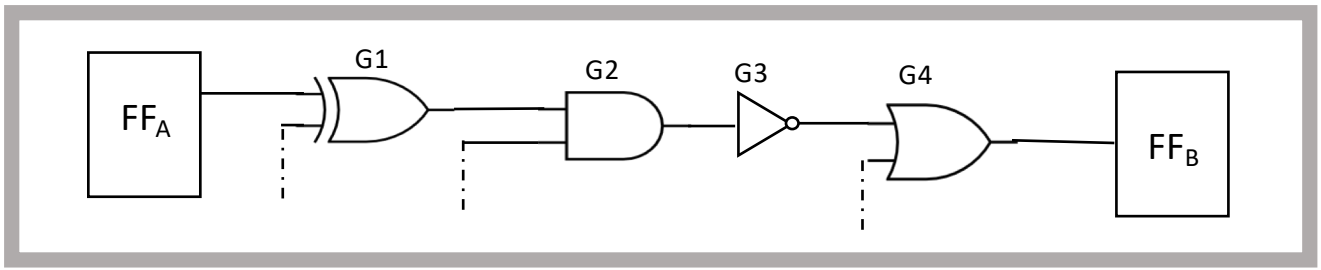


Single Event Transient Analyzer- SETA

- SETA tool phases:
- Load circuit nodes
  - Logic Functions and FFs
- Terminal nodes identification
- Sensitive nodes identification
- Execution of propagation for each
  - Generated SET pulse
  - Sensitive node



Terminal nodes are the destination points of SET propagation



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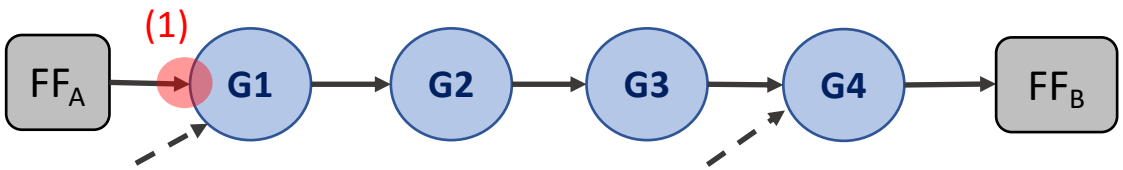
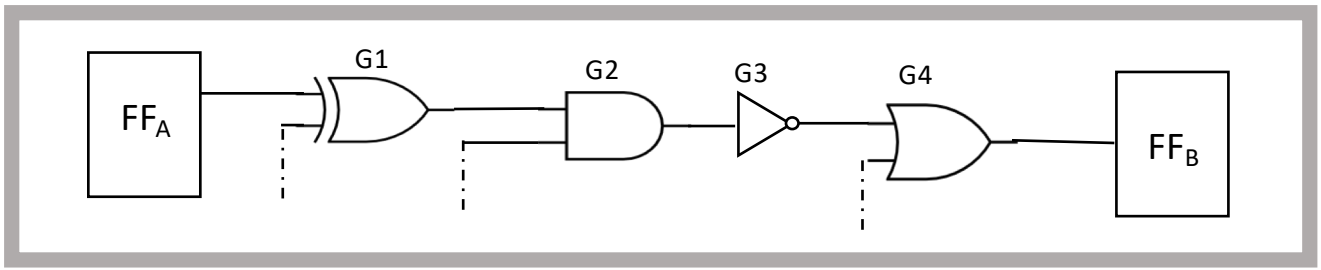


Injection [#]	Source SET [ns]	SET reach to FF [ns]
(1)	0.35	0.4



Single Event Transient Analyzer- SETA

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  - For each generated SET pulse
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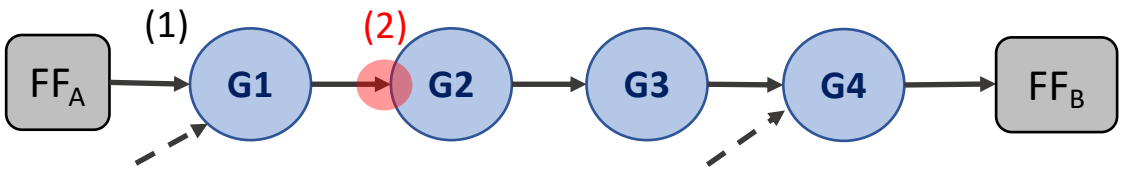
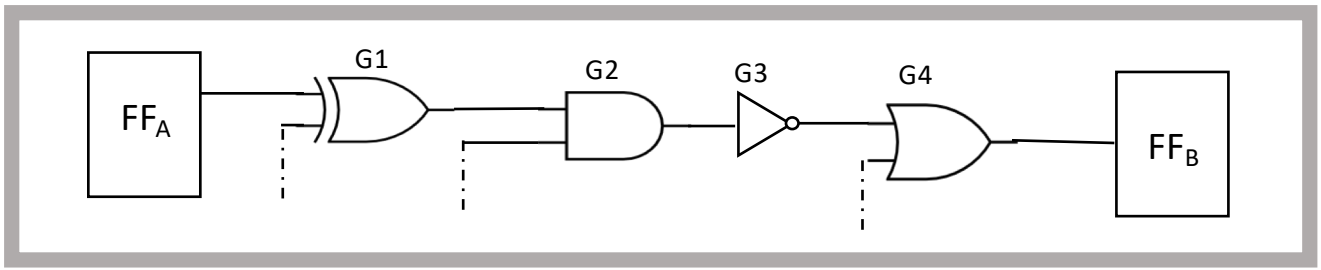


Injection [#]	Source SET [ns]	SET reach to FF [ns]
(1)	0.35	0.4
(2)	0.35	0.42



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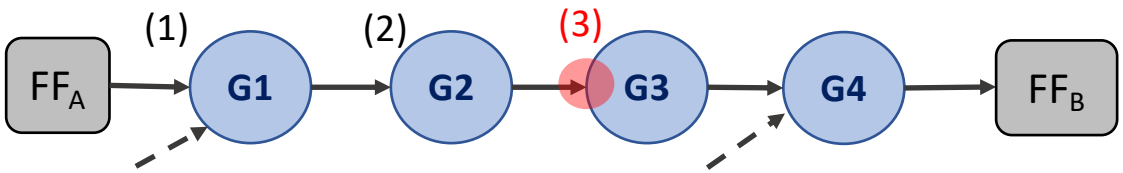
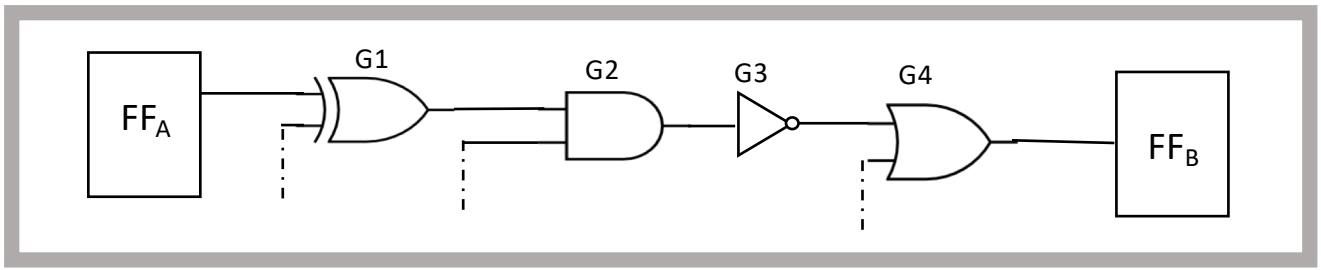
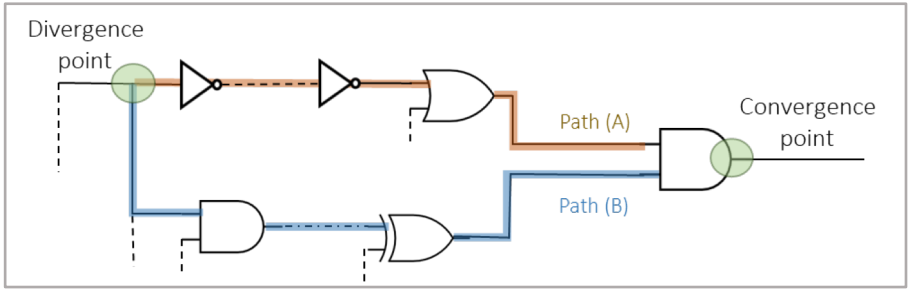


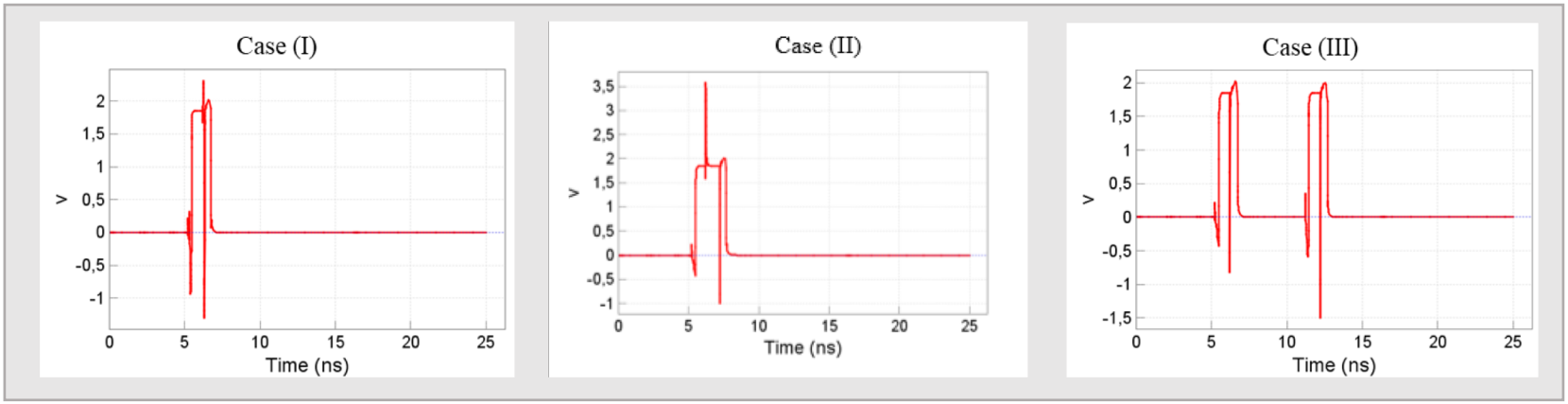
Injection [#]	Source SET [ns]	SET reach to FF [ns]
(1)	0.35	0.4
(2)	0.35	0.42
(3)	0.35	0.3
…	…	…

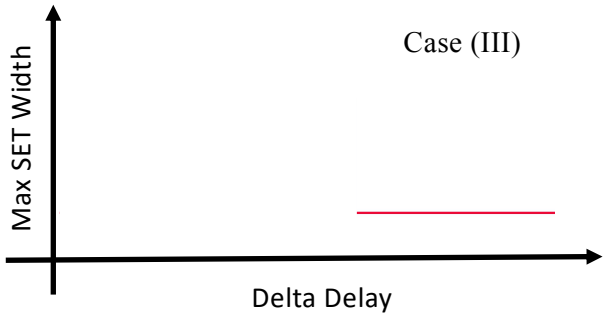


Single Event Transient Analyzer- Convergence SETA

- C-SETA: a CAD tool to evaluate the sensitivity of the implemented circuit regarding convergence SET







Single Event Transient Analyzer

- SETA and C-SETA applied to Flash-based FPGA
  - Microsemi A3P250 Flash-based FPGA
  - Injecting SET pulses less than 1 ns

Characteristics of the original benchmark circuits

Circuits	Versatile [#]	FFs [#]	Frequency [MHz]
B05	415	66	47
B09	493	67	46
B12	565	123	48
B13	162	50	52
CORDIC	956	240	45
RISC	1,401	1,156	42

Single Event Transient Analyzer

- SETA and C-SETA applied to Flash-based FPGA
  - Microsemi A3P250 Flash-based FPGA
  - Injecting SET pulses less than 1 ns

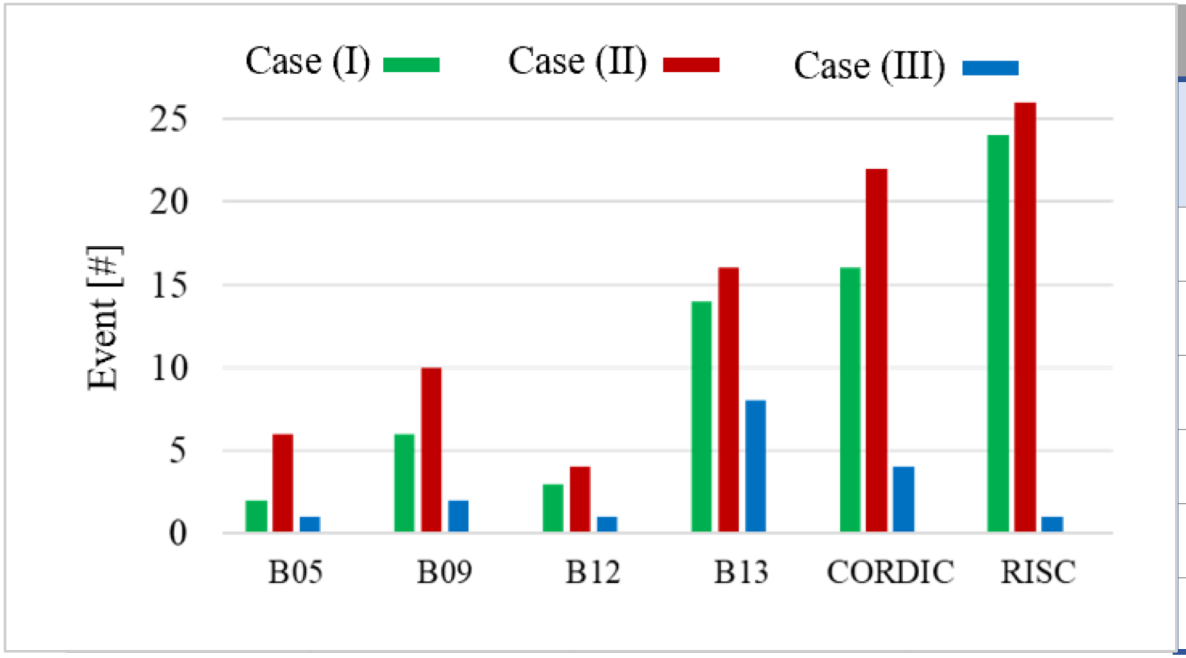
SET sensitivity analysis

Circuits	Filtered [#]	Partially Filtered [#]	Broadened [#]	C-SET [#]
B05	9	3	8	9
B09	3	6	11	18
B12	1	7	13	8
B13	14	8	7	38
CORDIC	12	28	39	42
RISC	204	184	196	56

Single Event Transient Analyzer

- SETA and C-SETA on Flash-based FPGA
  - Microsemi A3P250 Flash-based FPGA
  - Injecting SET pulses less than 1 ns

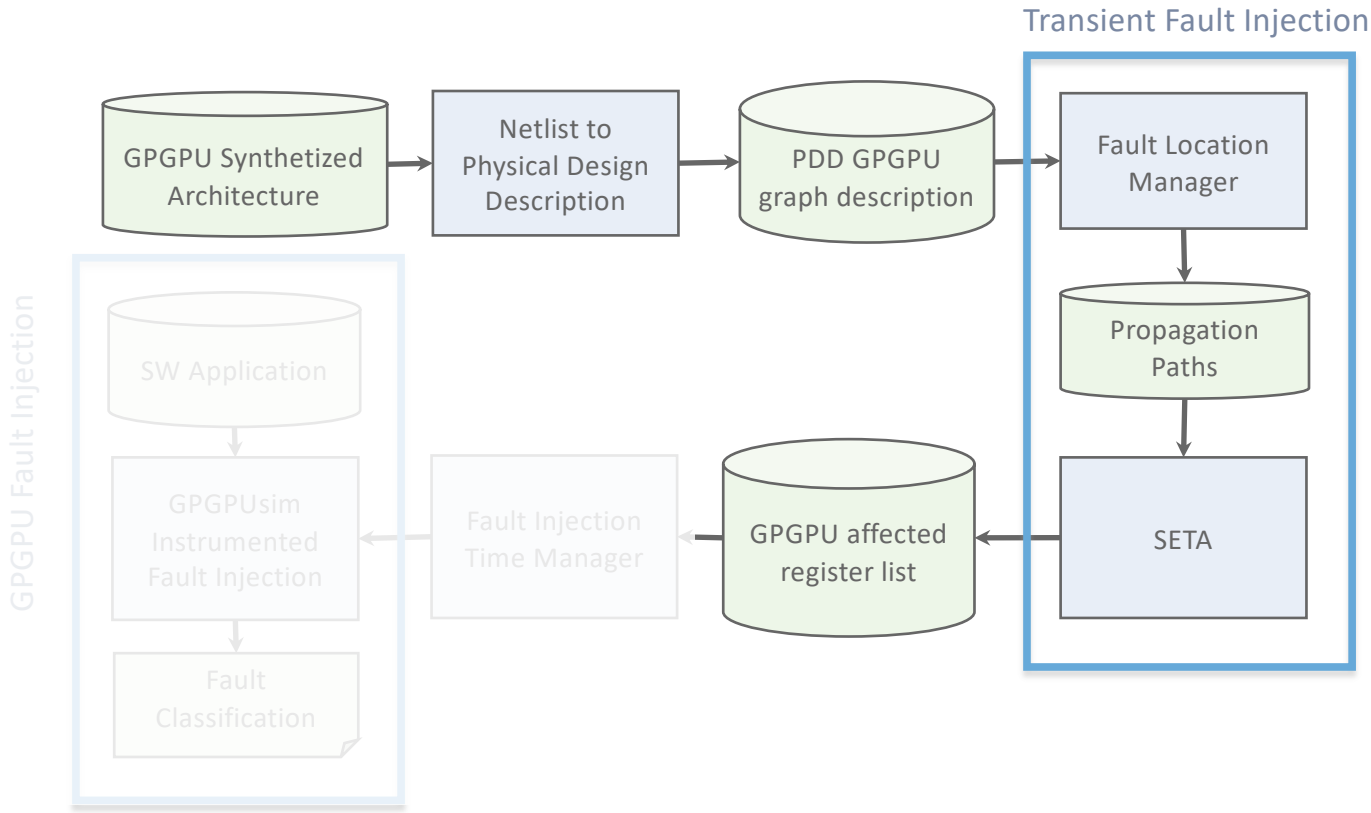
SET sensitivity analysis



C-SET [#]
9
18
8
38
42
56

Single Event Transient Analyzer- GPGPU

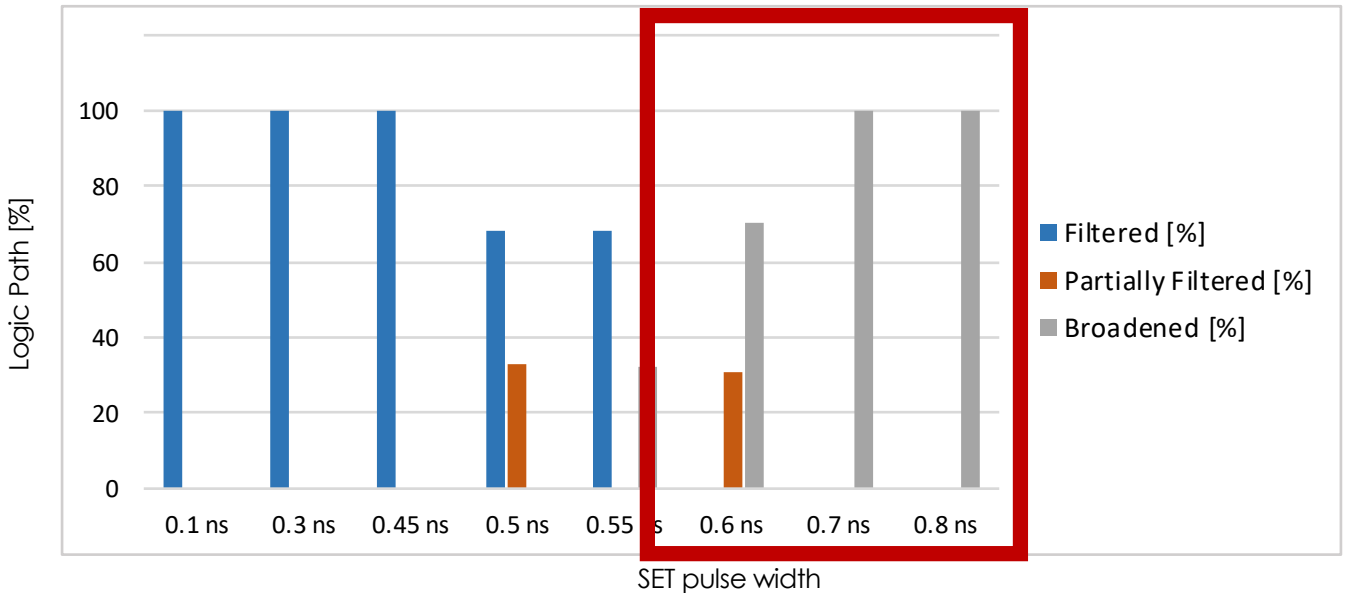
- SET on GPGPU
  - Simulation based environment (GPGPUsim) instrumented for Transient Fault Injection



S. Azimi, B. Du, L. Sterpone, "*Evaluation of Transient Errors in GPGPUs for Safety Critical Applications: An Effective Simulation-based Fault Injection Environment*", Journal of Systems Architecture, ISSN 1383-7621.

Single Event Transient Analyzer- GPGPU

- SET on GPGPU
  - NVIDIA G80 GPGPU model architecture using hardware model of the FlexGrip GPGPU
  - Using ProASIC3 Library for synthesizing of the SM model
  - Evaluating the sensitivity of a single streaming processor including 4K gates and 238K logical paths



Single Streaming processor SET sensitivity overview

S. Azimi, B. Du, L. Sterpone, "*Evaluation of Transient Errors in GPGPUs for Safety Critical Applications: An Effective Simulation-based Fault Injection Environment*", Journal of Systems Architecture, ISSN 1383-7621.

Mitigation of SET

- Mitigation solutions for the SET phenomenon are based on:
  - Redundancy, such as TMR
    - Introducing DELAY, POWER and AREA OVERHEAD
  - Inserting SET filtering and Guard-Gate for all the user memory or Flip-Flop resources

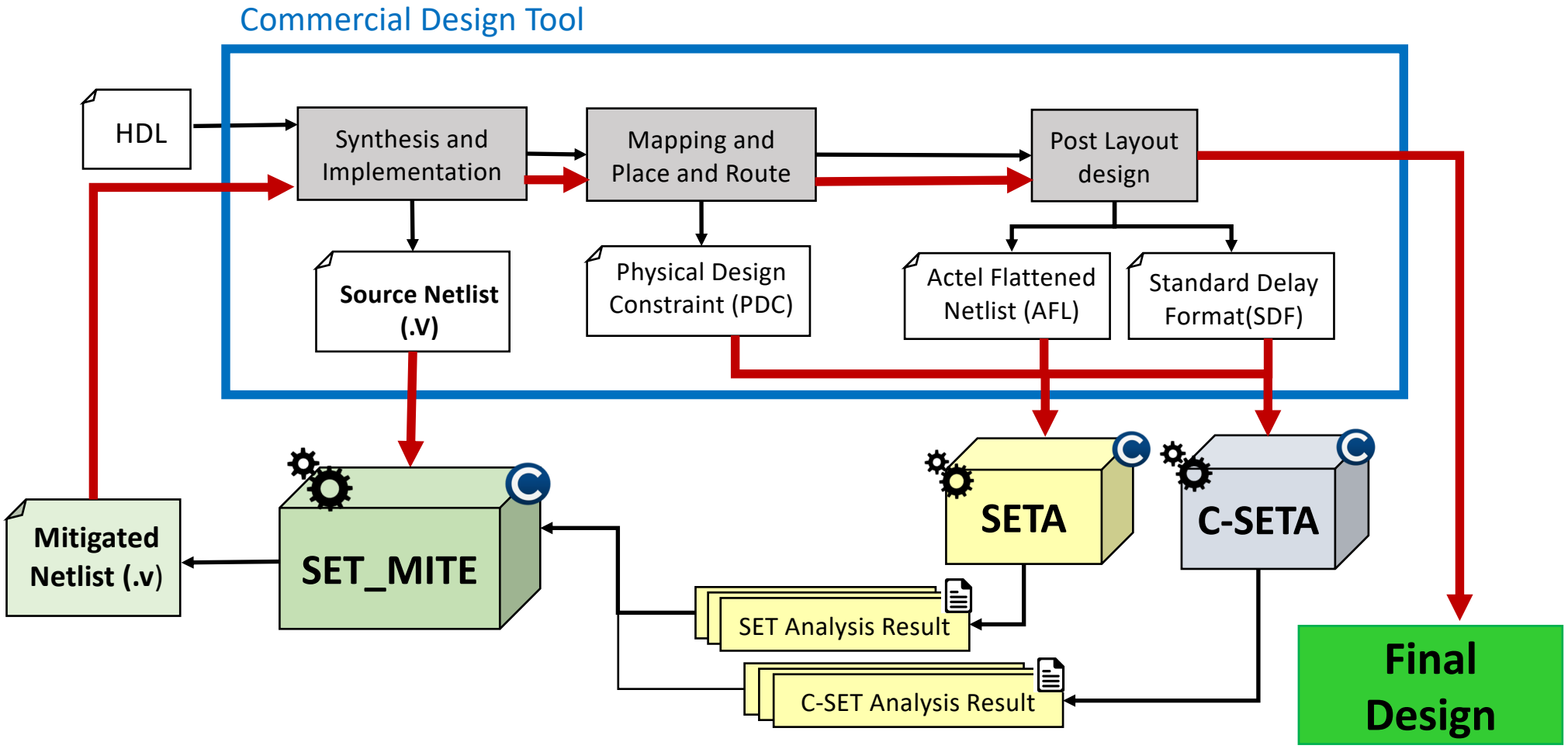
Mitigation of SET

- Mitigation solutions for the SET phenomenon are based on:
  - Redundancy, such as TMR
    - Introducing DELAY, POWER and AREA OVERHEAD
  - Inserting SET filtering and Guard-Gate for all the user memory or Flip-Flop resources

- For mitigating SET affecting Flash-based FPGAs, two solutions are proposed:
  - Applying filtering Guard Gate logics to the sensitive points of the circuits
    - Timing and area overhead
  - Mitigating by adding Charge Sharing logics to the sensitive points of the circuits
    - Zero timing overhead

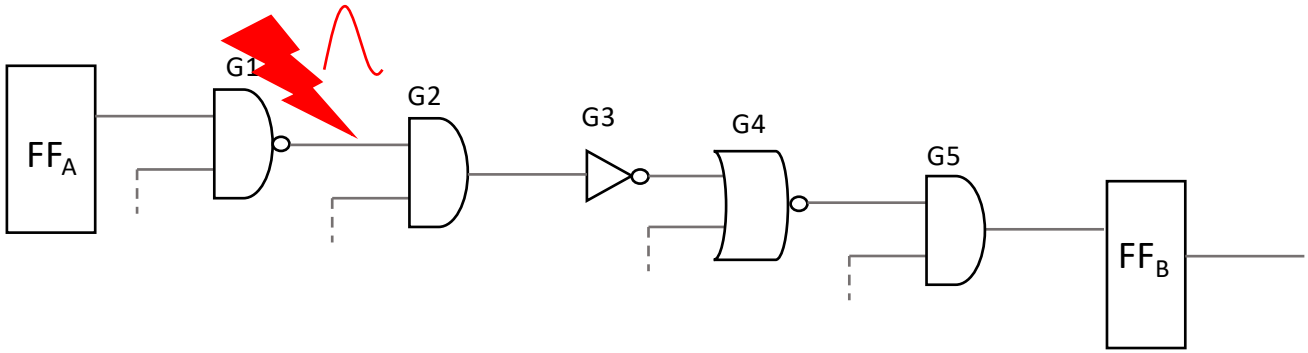
Mitigation of SET - Guard Gate Filtering Logic

- Mitigation of Single Event Transient



Mitigation of SET - Guard Gate Filtering Logic

- SET_MITE modifies a netlist according to SETA report
  - Inserting a Guard Gate logic structure on the input of the selected FF



Flip-Flop	Source_SET [ns]	SET each to FF [ns]
FF_B	0.35	0.42

Mitigation of SET - Guard Gate Filtering Logic

- SET_MITE modifies a netlist according to SETA report
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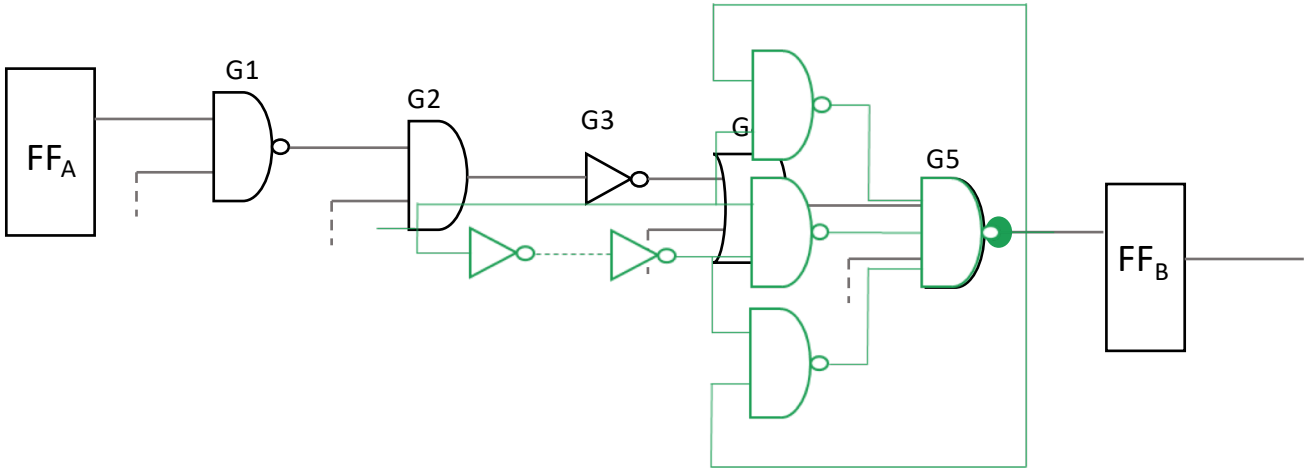

Flip-Flop	Source_SET [ns]	SET each to FF [ns]
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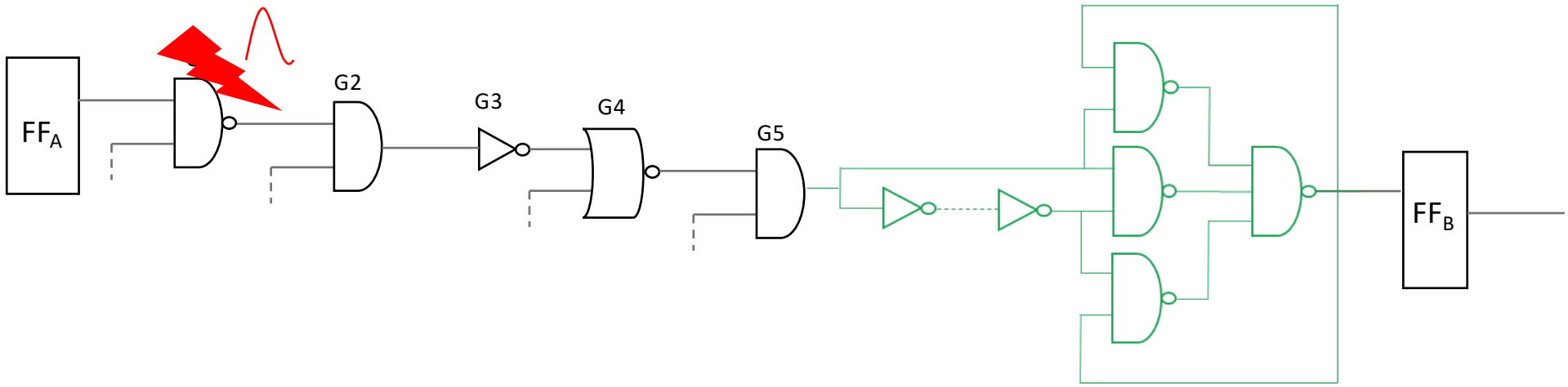

Flip-Flop	Source_SET [ns]	SET each to FF [ns]
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Mitigation of SET - Guard Gate Filtering Logic

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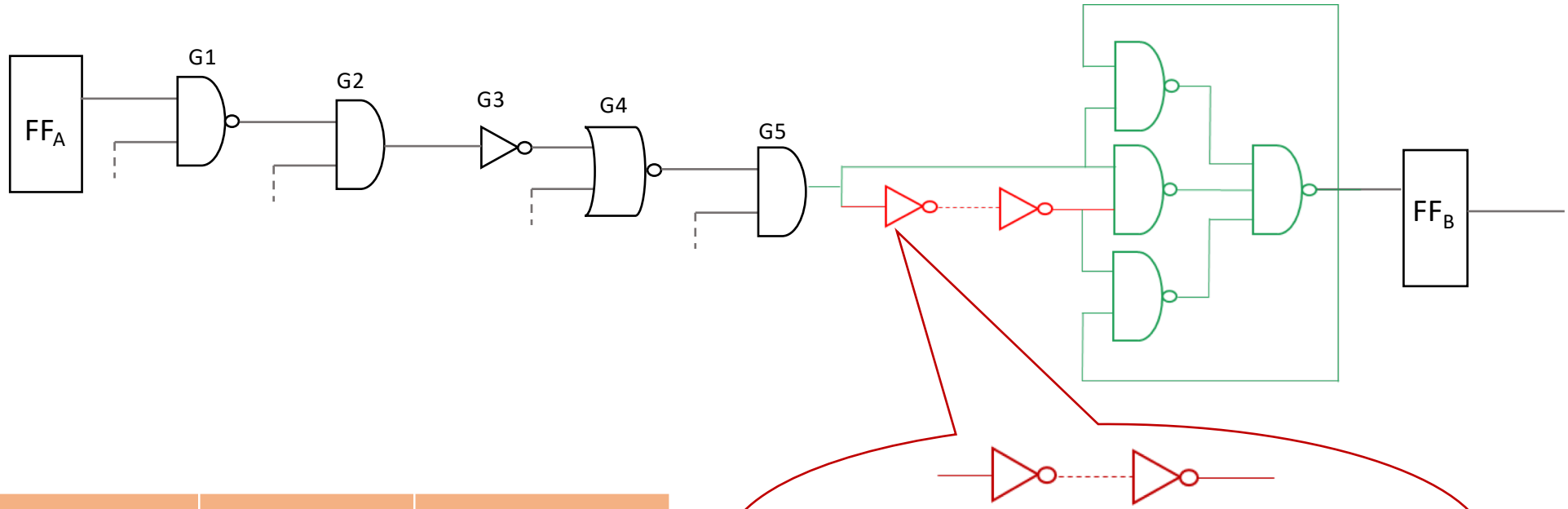


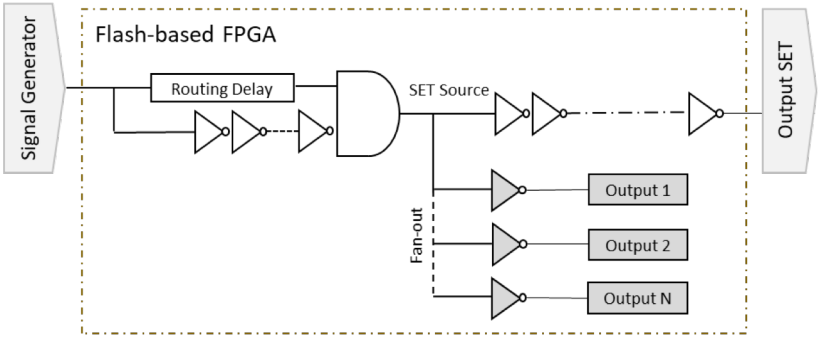
Flip-Flop	Source SET [ns]	SET reach to FF [ns]
FF$_B$	0.35	0.42

Calculation of SET filtering delay with respect to max SET pulse reported by SETA

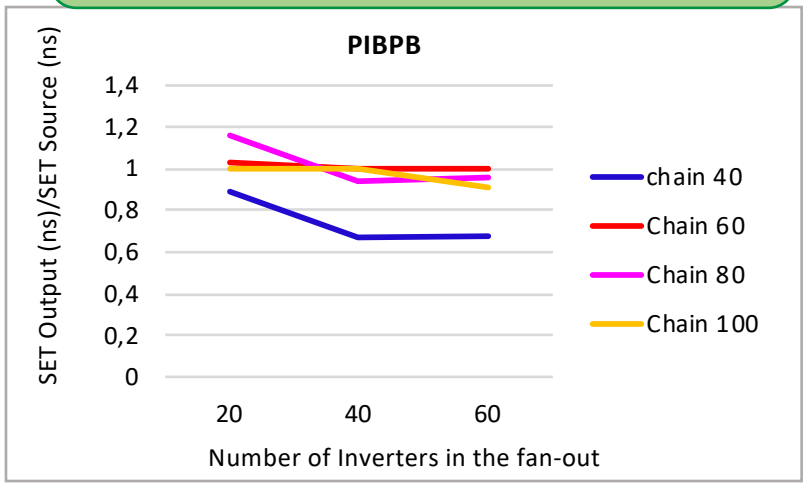
Azimi. S, Du. B, Sterpone. L, Merodio. D, Grimoldi. R, "*Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs*", ACM Great Lake Symposium on VLSI (GLSVLSI), 2017.

Mitigation of SET - Charge Sharing Filtering Logic

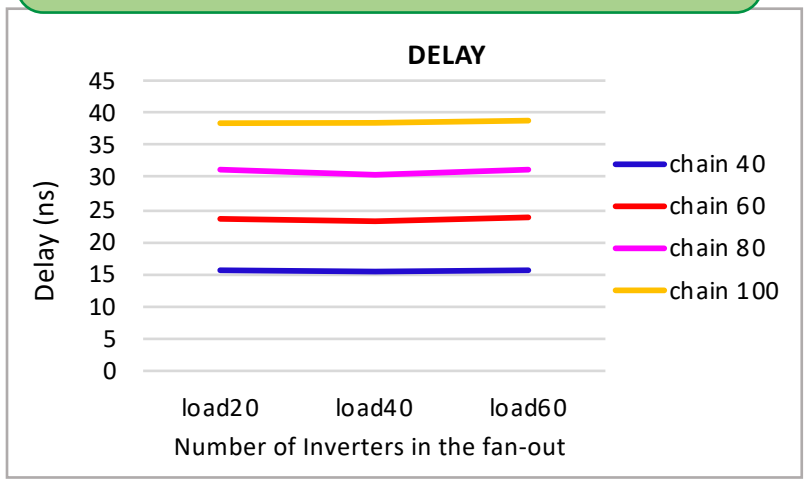
- Developing a SET mitigation algorithm based on inserting Charge Sharing logic:



Attenuating of PIPB by increasing of Fanout



By increasing the fanout, the delay of the circuit is not changing



Mitigation of SET - Charge Sharing Filtering Logic

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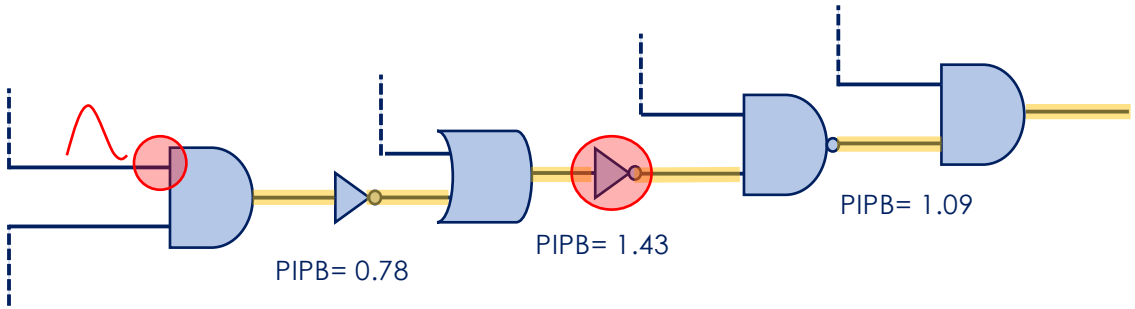
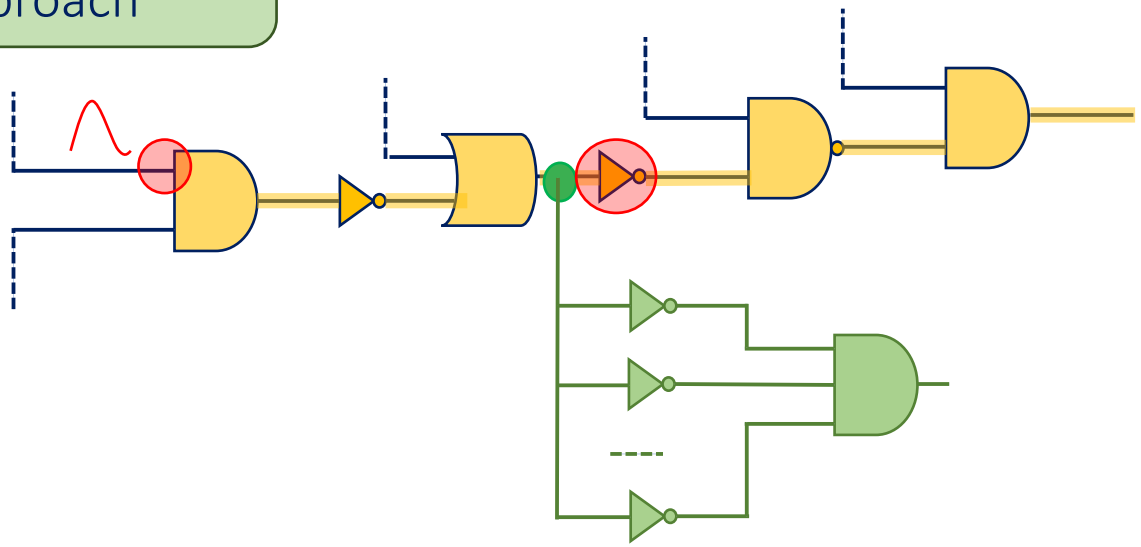


Mitigation of SET - Charge Sharing Filtering Logic

- Developing a SET mitigation algorithm based on inserting Charge Sharing logic:
  - Selecting the suitable nodes for the charge sharing logic insertion based on the performed SET analysis
  - Modifying the place and route by inserting the mitigation gates
  - Distributing the charge collection, reducing the amplitude and width of the SET pulse

Zero-Timing Overhead SET Mitigation Approach



Azimi. S, Du. B, Sterpone. L, "*On the Mitigation of Single Event Transients on Flash-based FPGAs*" ,23rd IEEE European Test Symposium (ETS), 2018.

Single Event Transient Analyzer

- Mitigation Flash-based FPGA
  - A3P250 flash-based FPGA
  - Injecting SET pulses less than 1 ns

SET fault injection wrong answer comparison for 5000 SETs lower than 1 ns

Circuits	Wrong Answers [%]		
	Plain	Guard-Gate	Charge Sharing
B05	68.5	12.2	4.3
B09	72.6	8.4	2.6
B12	83.2	9.4	3.1
B13	54.8	16.5	4.1
CORDIC	89.4	19.6	4.3
RISC	94.6	21.6	4.8

Timing and Area overhead for each method

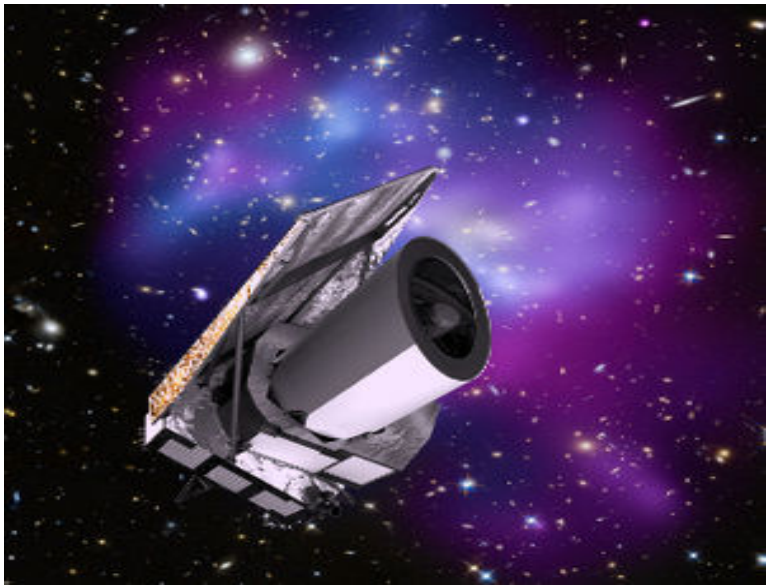
Circuits		B05	B09	B12	B13	CORDIC	RISC
Timing [%]	Guard Gate	12	13	15	16	19	18
	Charge Sharing	0	0	0	0	0	0
Area [%]	Guard Gate	27	28	28	27	32	31
	Charge Sharing	25	27	25	24	28	27

Mitigation of Single Event Transient

Basic Mechanism	Application	Industrial
Modelization Characterization	Tools and Algorithm for Analysis and Mitigation	EUCLID Space Mission Project

EUCLID

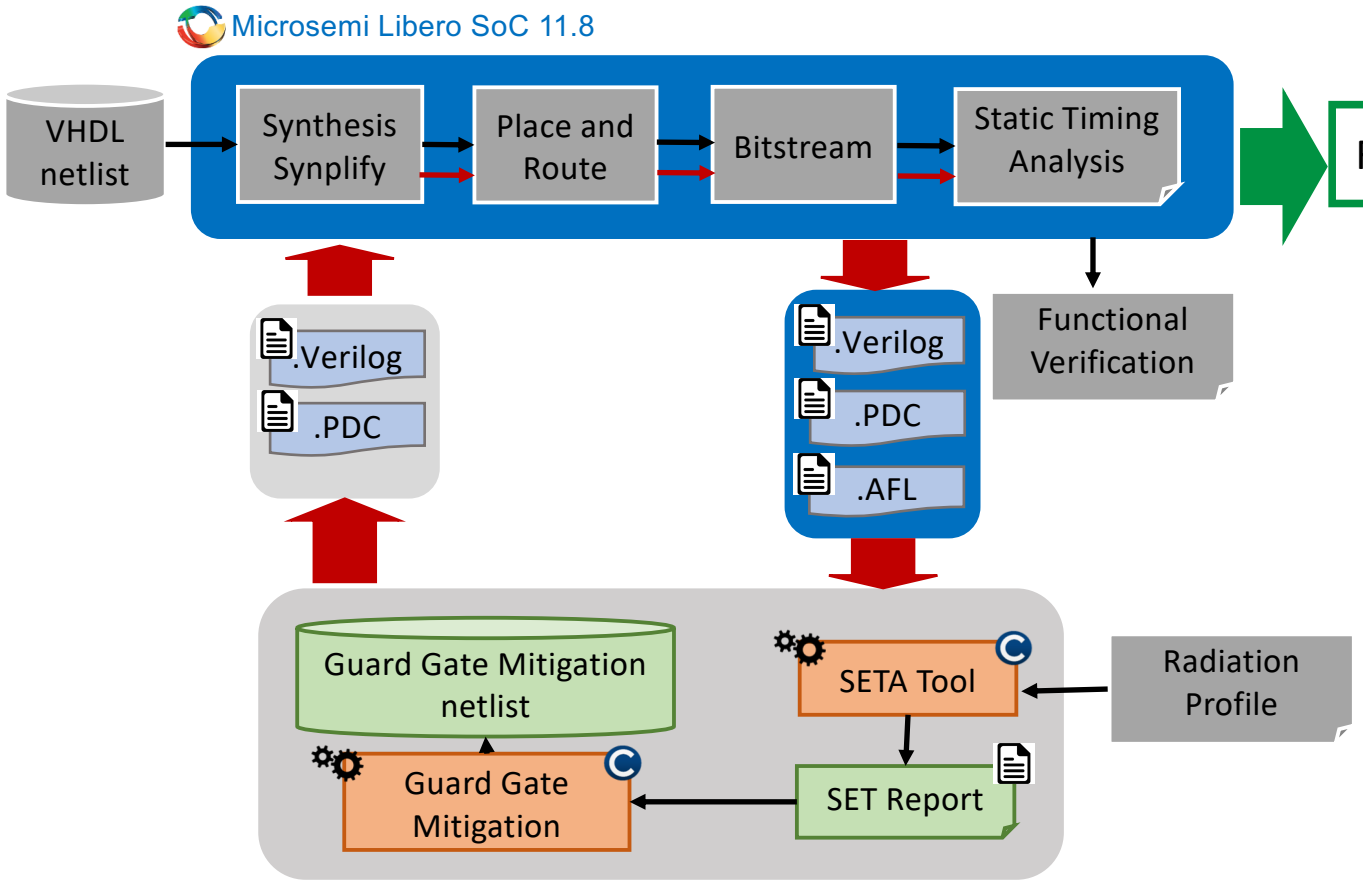
- EUCLID Space Mission
  - Objective: To study the geometry and nature of dark universe
  - Normal duration of the mission: 6.25 years
  - Launch: Planned for 2020
  - Radiation mission profile
    - Maximum exposure of 4 Krad
    - SETs duration between 0.43 ns and 0.45 ns
  - Microsemi ProASIC3 A3P3000 Flash-based FPGA
  - Microsemi Libero SoC design tool



EUCLID space craft

EUCLID

- SET analysis and mitigation flow on EUCLID



Politecnico di Torino
SEE-aware design flow

EUCLID

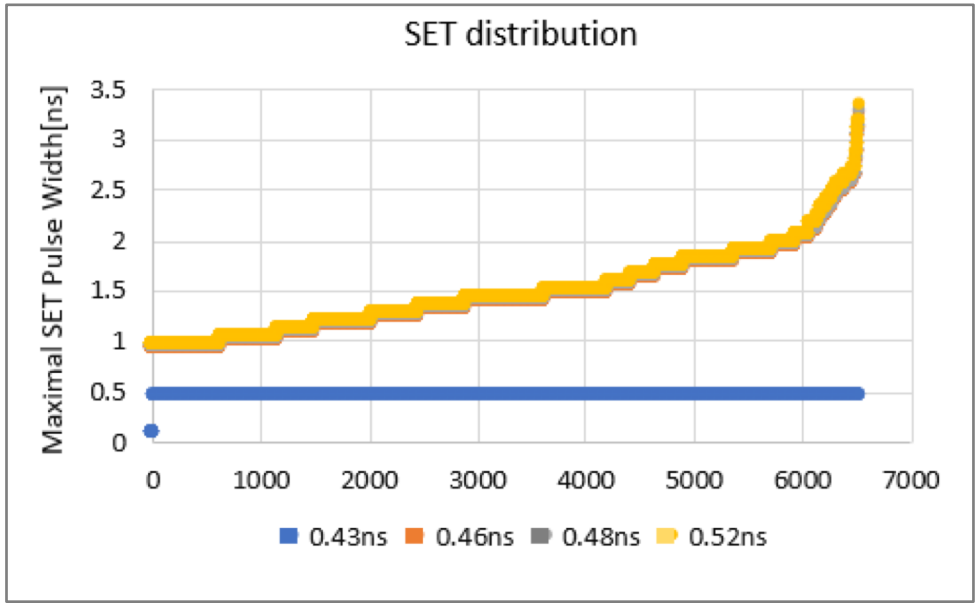
- Performing SET sensitivity analysis on EUCLID original netlist
- Source SET pulses width range from 0.43 to 0.52 ns

EUCLID Circuit Recourses

Type	CoreTiles [#]
Combinational Logic	30,190
Flip – Flops	17,718

SET analysis for SET Ranging from 0.43 ns to 0.52 ns representing the number of Flip-Flops for each case

Source SET [ns]	Totally Filtered [#]	Partially Filtered [#]	Broadened [#]
0.520	11,130	0	6,452
0.488	11,130	0	6,542
0.4462	11,130	0	6,541
0.437	11,162	6,510	0



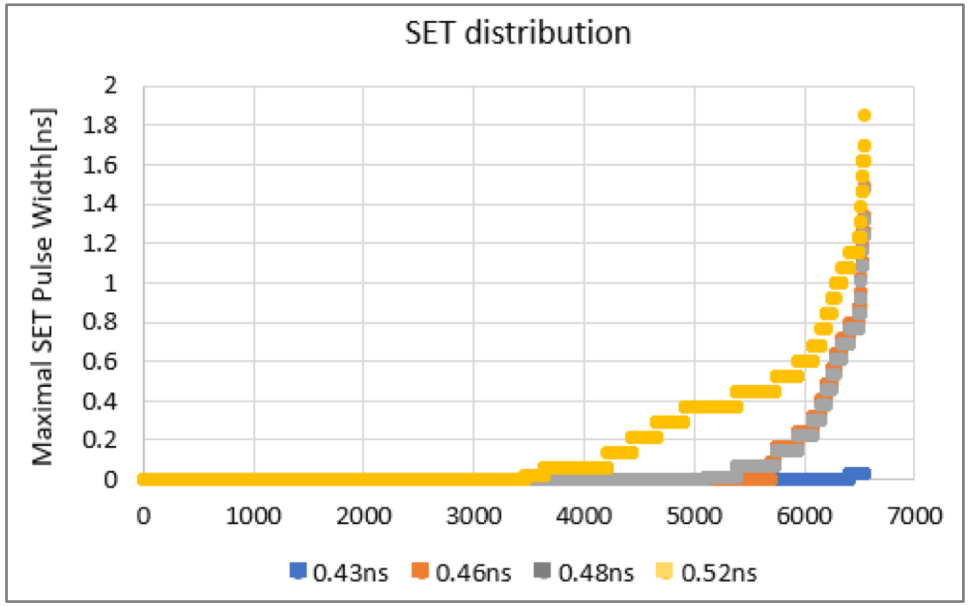
SET distribution on the **original** EUCLID netlist

Azimi. S, Du. B, Sterpone. L, Merodio. D, Grimoldi. R, "*Effective Mitigation of Radiation-induced Single Event Transient on Flash-based FPGAs*", ACM Great Lake Symposium on VLSI (GLSVLSI), 2017.

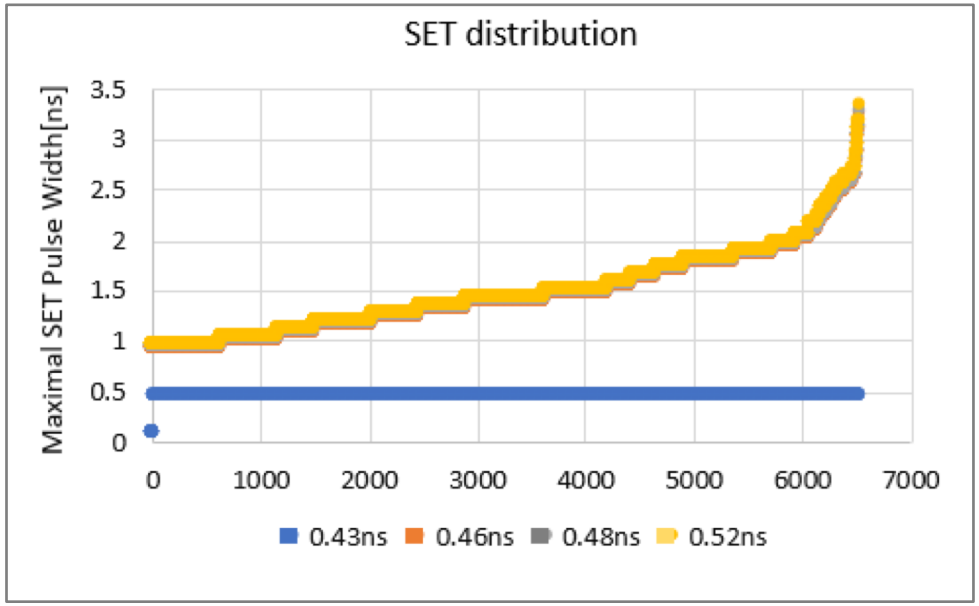
EUCLID

- Automatically inserting a Guard Gate structure at the input of a Flip-Flop candidate to SET filtering
  - SET mitigation comparison between original netlist and mitigated netlist
    - Removal of 97%
    - Remaining 3%

Space Product Assurance Techniques for radiation effects mitigation in ASICs and FPGAs handbook

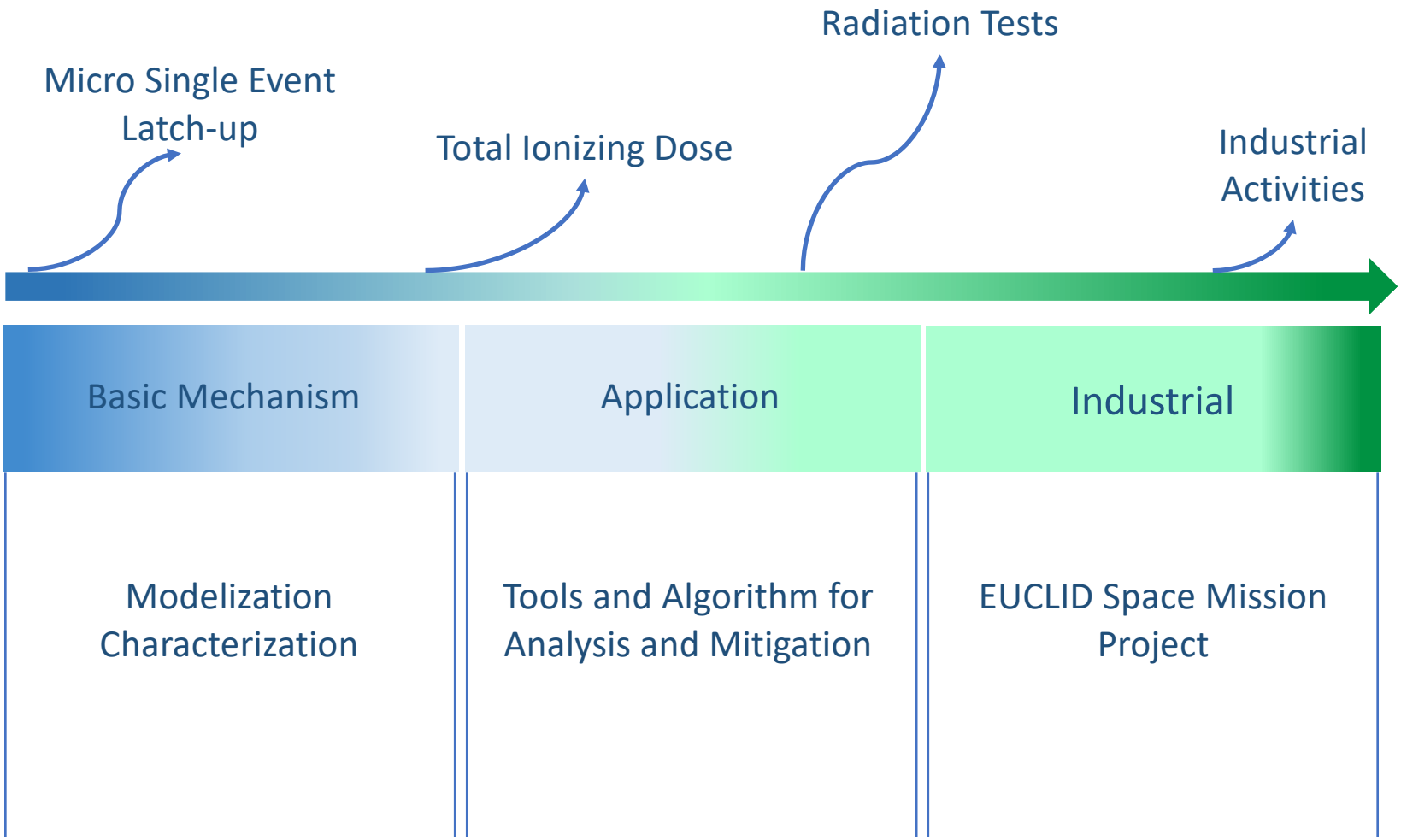


SET distribution on the **mitigated** EUCLID netlist



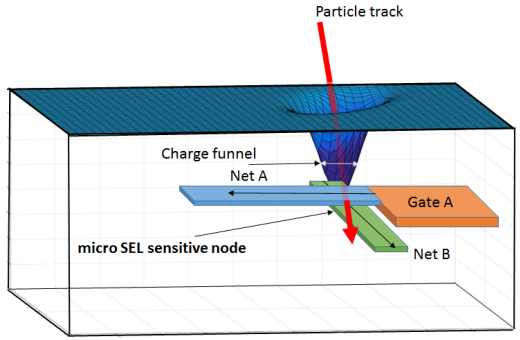
SET distribution on the **original** EUCLID netlist

Complementary activities



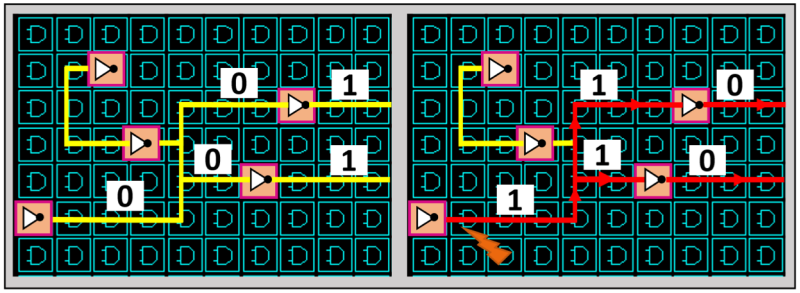
Micro Single Event Latch up

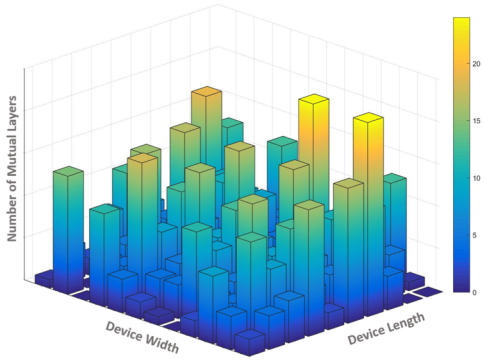
- Micro Single Event Latch-up
  - Localized Latch up current representing a small fraction of the normal overall integrated circuit current
  - Generated by particle strike (even with low energy)
  - Enabling bits to change state within a given region



Generation of micro SEL on the output of the gate

- Evaluating the sensitivity of the design under the test
  - Placement and routing architecture within the physical layer mapping
  - Calculating the realistic micro SEL occurrence



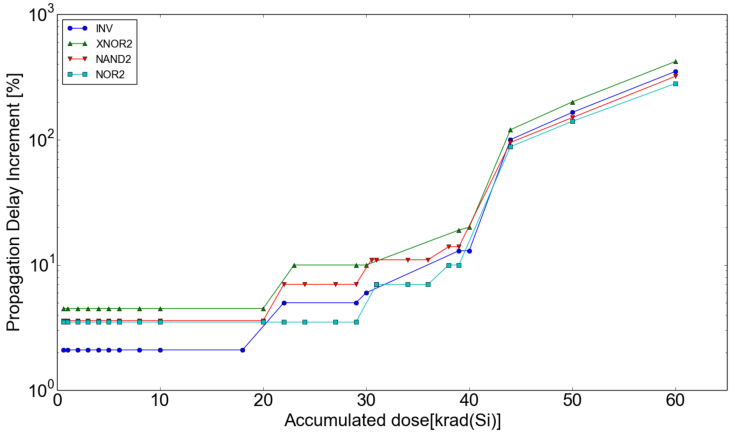


Layer distribution of the routing architecture with respect to number of layers shared the mutual location

Azimi. S, Sterpone. L, "*Micro Latch-up Analysis on Ultra- Manometer VLSI Technologies: A new Monte Carlo Approach*", IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2017.

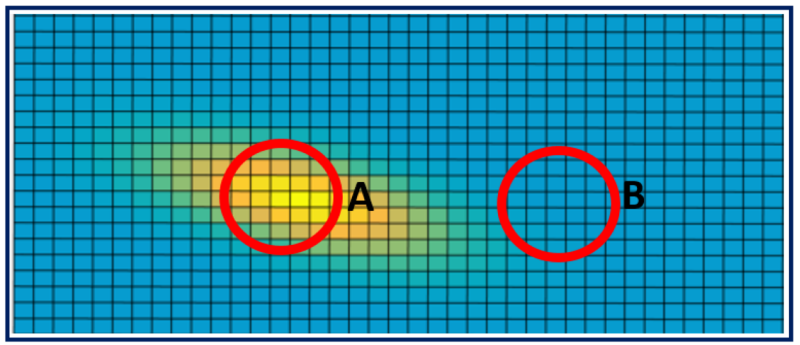
Total Ionizing Dose

- Effect of accumulation of the charge imposed by particles causing misbehavior of the system
  - Slowing down the transistors
  - Increasing of power consumption
  - Increasing the sensitivity of the system regarding SEU



Performance degradation for different types of gates

- Total Ionizing Dose analysis methodology
  - Modeling the performance degradation
  - TID effect distribution model
  - Simulation based environment for error rate report



Heatmap generation considering TID distribution

C. Q. Zhang, **S. Azimi,** G. L. Vaccara, L. Sterpone, B. Du, "*A New Approach for Total Ionizing Does Effect Analysis on Flash-based FPGA*", Microelectronics Reliability, 2017.

Radiation tests

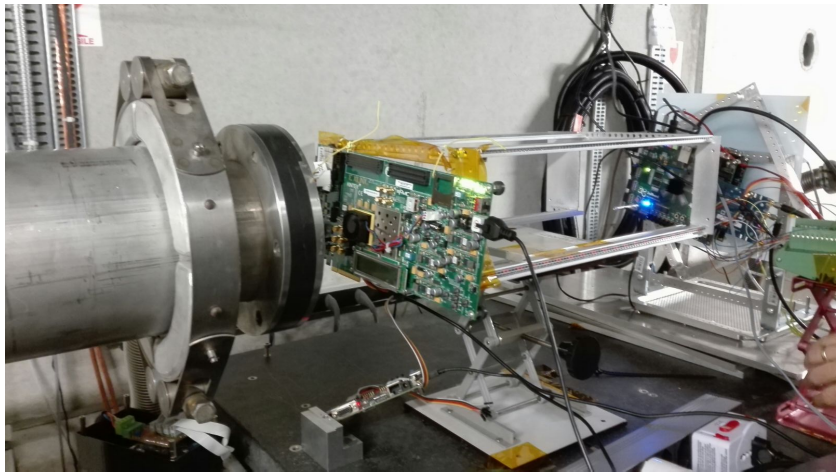
- Ultra high energy heavy ion test beam on Xilinx Kintex7 SRAM-based FPGA and Microsemi ProASIC3 Flash-based FPGA – CERN

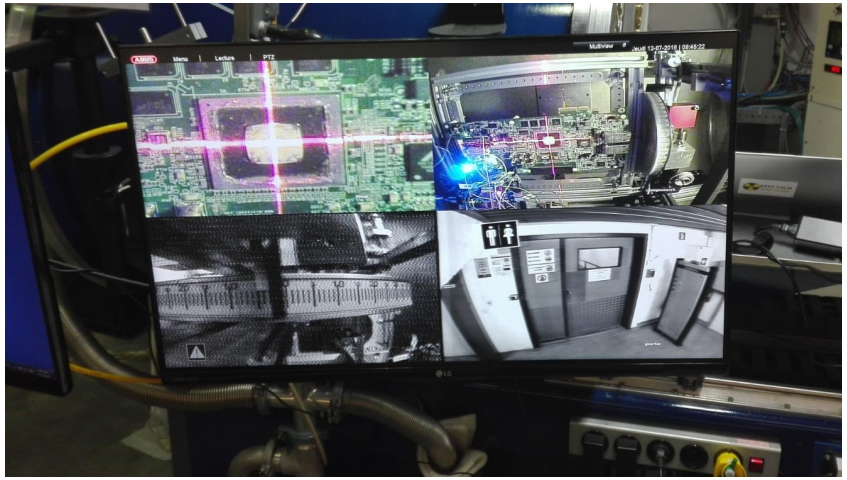
Azimi. S, Du. B, Sterpone. L, Codinachs. D, Cavrios. V, Polo. C, Alia. R, Kastriotou. M, Martinez. P, "*Ultra High Energy Heavy Ion Test beam on Xilinx Kintex7 SRAM-Based FPGA*",In: Transaction on Nuclear Science 2019.

- Heavy Ion test on Microsemi **Smartfusion2 Flash-based FPGA** – UCL
- Heavy Ion test on **Xilinx UltraScale+ SRAM-based FPGA** - UCL

Sterpone. L, **Azimi. S,** Bozzoli. L, Du. B, Lange. T, Glorieux. M, Alexandrescu. D, Boatella. P, Codinachs. D, "*A Novel Error Rate Estimation Approach for UltraScale+ SRAM-based FPGAs*", In: 12th NASA/ESA Conference on Adaptive Hardware and Systems (AHS), 2018.

- Heavy Ion test on Microsemi **Smartfusion2 Flash-based FPGA** - UCL





Industrial Activities

- General Motors
  - Development of Software testing framework with a Virtual Hardware prototyping tools
    - Developing a SW test framework containing test manage and infrastructure toward virtualizing environment

Azimi. S, Moramarco, A; Sterpone, L, "*Reliability evaluation of heterogeneous systems-on-chip for automotive ECUs*" In: IEEE 26th International Symposium on Industrial Electronics (ISIE), 2017.

- European Space Agency
  - Single Event Effects analysis and mitigation on SRAM and Flash-based FPGAs
    - Developing an efficient software tool for analyzing Single Event Transient sensitivity of the circuit under the test

Azimi. S, Du. B, Sterpone. L, Codinachs, D. M, Cattaneo. L."*SETA: A CAD Tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs*" , In: 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), 2018.

- OHB Italia
  - In the framework of EUCLID project for evaluating transient error

Azimi. S, Du. B, Sterpone. L, Codinachs, D. R, Grimoldi. "*A new CAD tool for Single Event Transient Analysis and Mitigation on Flash-based FPGAs*" , In: Integration, the VLSI Journal, 2019.

Publication Summary

- **8 Journal papers**
  - IEEE, ACM, Elsevier
    - IEEE Access, IEEE TNS, Integration on VLSI, Microelectronic Reliability, Journal of Systems Architecture
- **16 Conference papers**
  - IEEE, ACM International Conferences
    - ARCS, DDECS, RADECS, ETS, DATE, ISVLSI, SMACD, AHS, GLSVLSI, ISIE,

Awards

Second prize in

"My Research in three minutes"

Granted 1000 EUR – Nov 2017

First prize in

"Best EDA Tool for improving design automation for integrated circuits and systems"

"IEEE Council on Electronic Design Automation"

Granted 1000 USD – Jul 2018

"Quality Award for Best PhD Students"

Granted 1200 EUR – Sep 2018

Thank you for your attention!

4th Space FPGA User Workshop – European Space Agency